半導体微細加工における プラズマ応用について

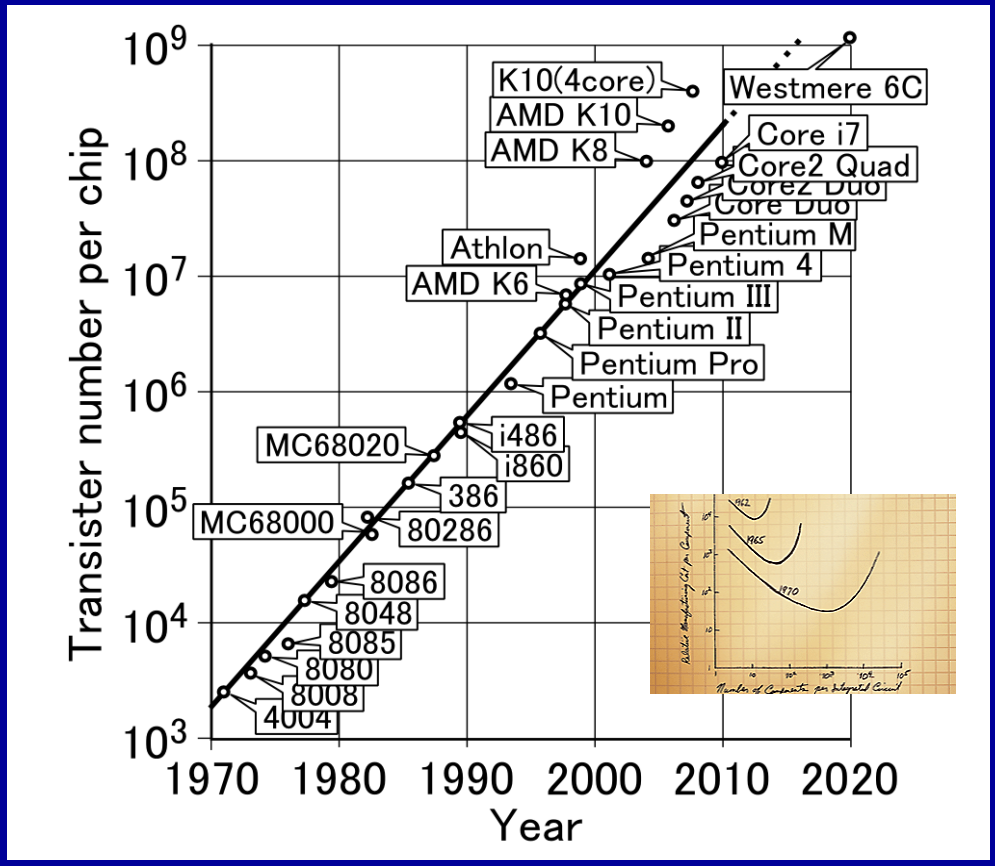
2017.12.22　原子分子データ応用フォーラムセミナー
特別セッション「半導体製造・プラズマプロセスと原子分子過程・分光研究とのかかわり」

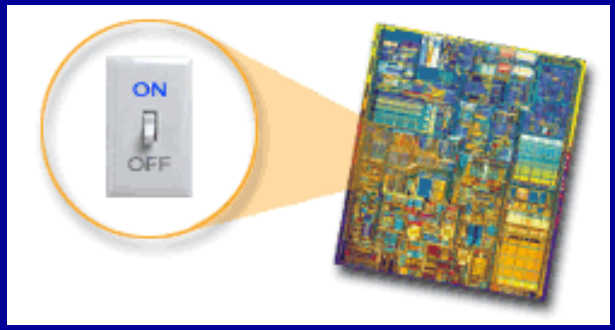
Tetsuya Tatsumi
Sony Semiconductor Solutions Corporation

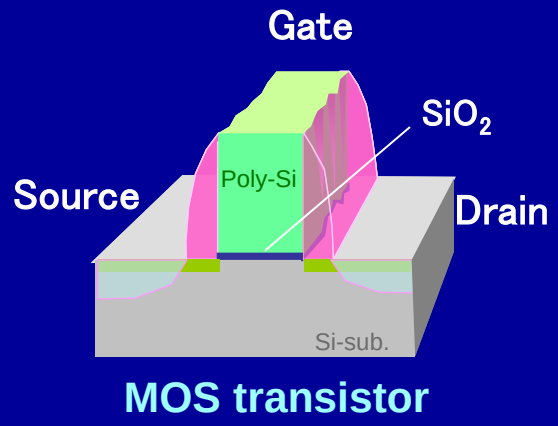
Outline

1. Introduction
2. High etch rate & Selectivity
3. Suppression of CD variation
4. Minimization of plasma induced damage
5. Summary

Moore's Law



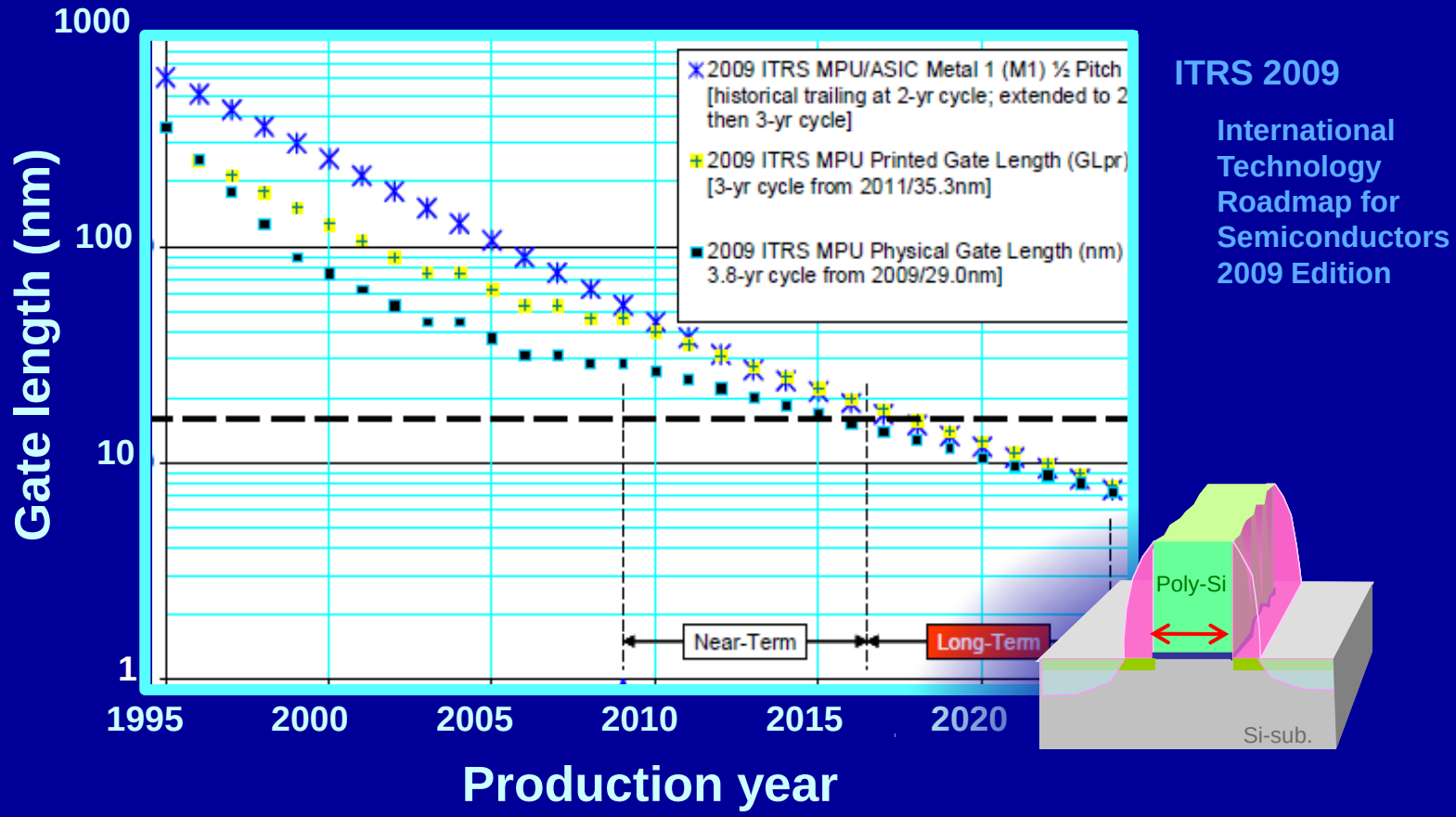




MOS transistor

Number of transistors increased exponentially

Transistor size



ITRS 2009

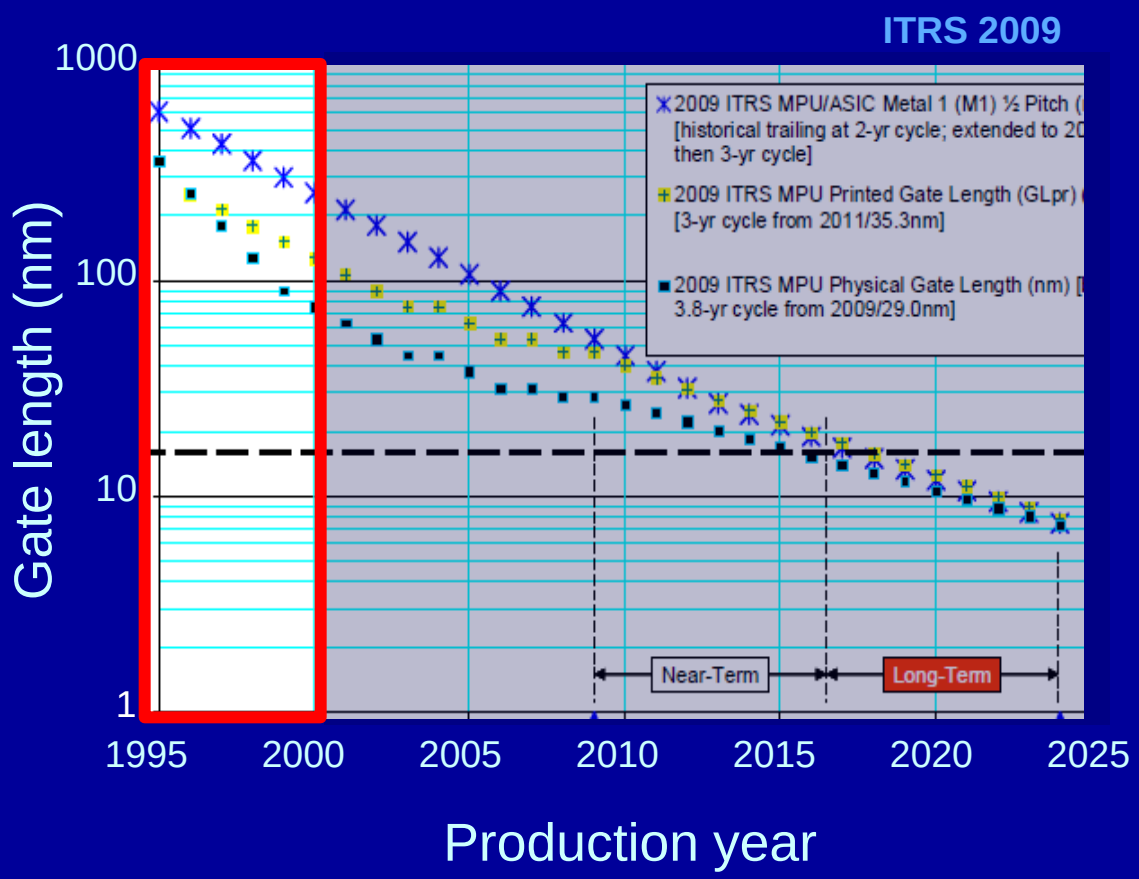
International Technology Roadmap for Semiconductors 2009 Edition

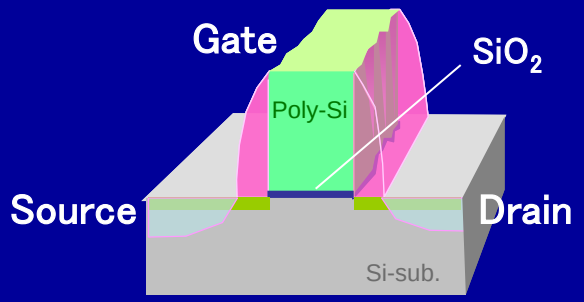
Requirement of plasma technologies for miniaturization of transistors

Outline

1. Introduction
2. 1990～ : High etch rate & Selectivity
3. 2000～ : Suppression of CD variation
4. 2010～ : Minimization of damage
5. Summary

Requirements (1990～)

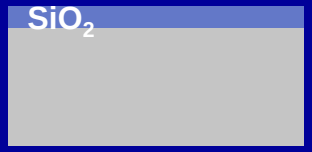




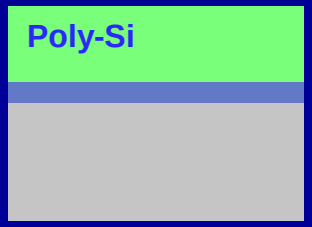
Gate length > 100nm
Anisotropic profile
High etch rate
High selectivity
100-200mmϕ wafer

Process flow

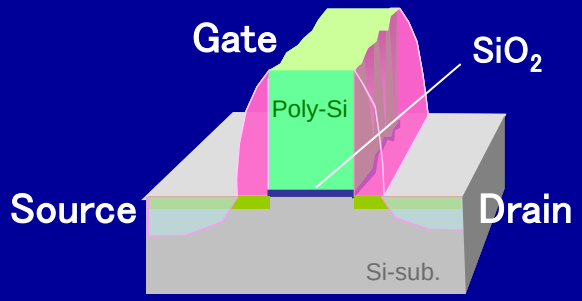
Si-substrate

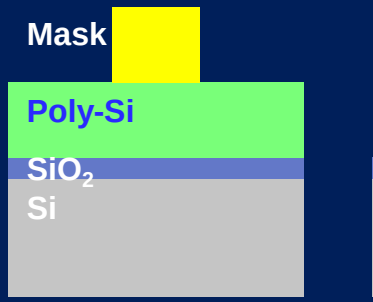


Gate SiO_2

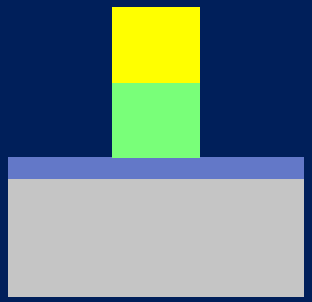


Doped poly-Si

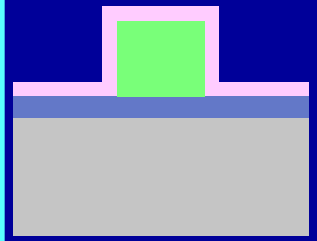




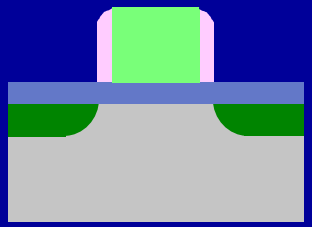
Resist mask



Plasma etching



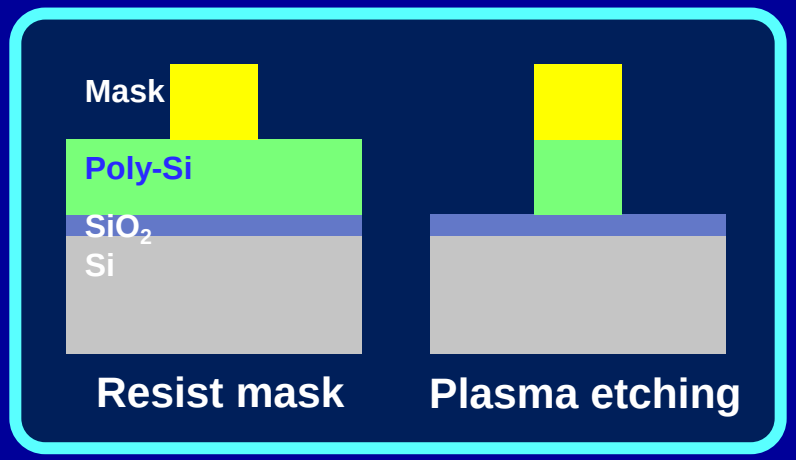
SiO_2 deposition

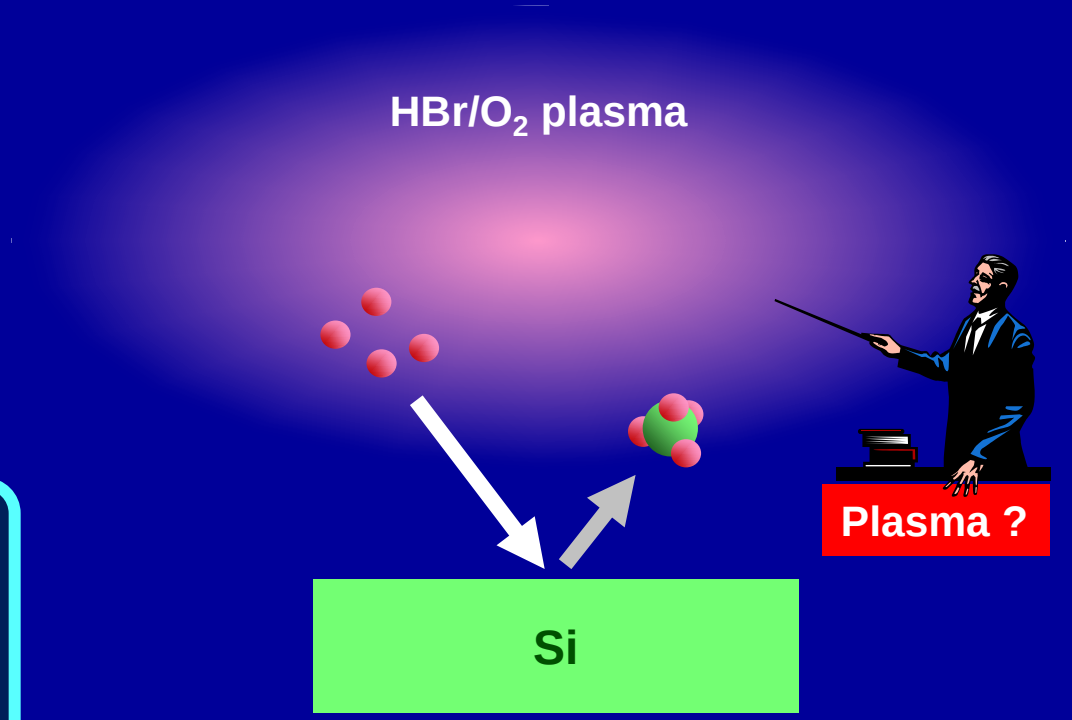


Etch back
& Doping

Surface reaction of Si etching

	B.P.
Si	2700℃
$SiBr_4$	154℃
$SiCl_4$	58℃
SiF_4	-86℃



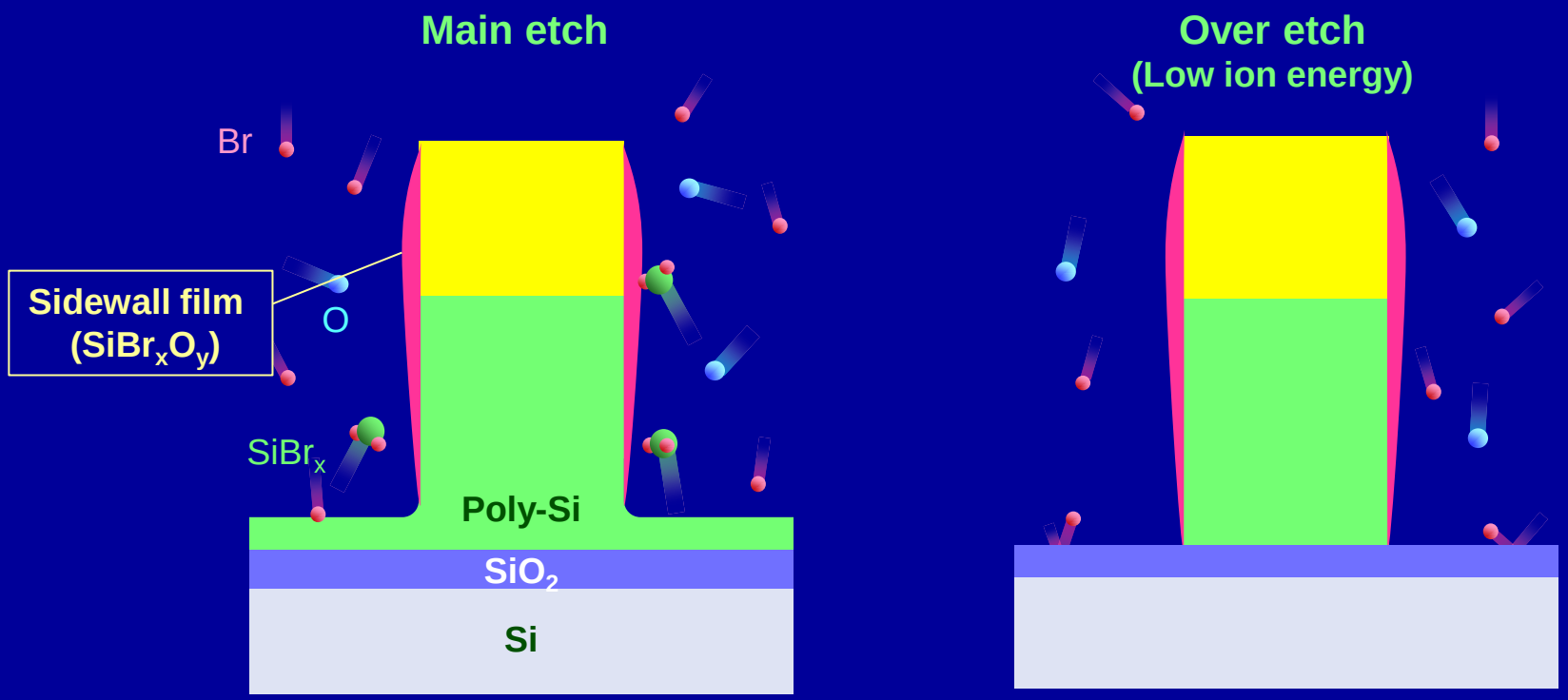


$Si\,(solid) + 4Br\,(gas) \rightarrow SiBr_4\,(gas)$

Dry etching of poly-Si gate on thin oxide film

Dry etching system

Surface reaction of Si etching



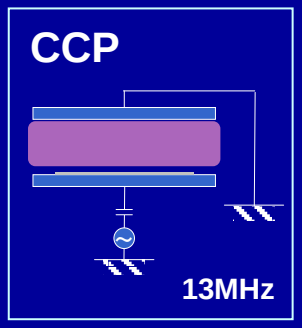
Binding energy:

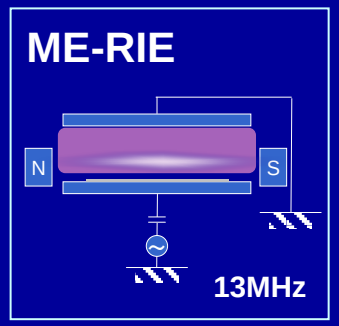
Si-Si < Si-Br < Si-O

Sidewall film ➔ Anisotropic profile

Low ion energy ➔ High selectivity to SiO_2

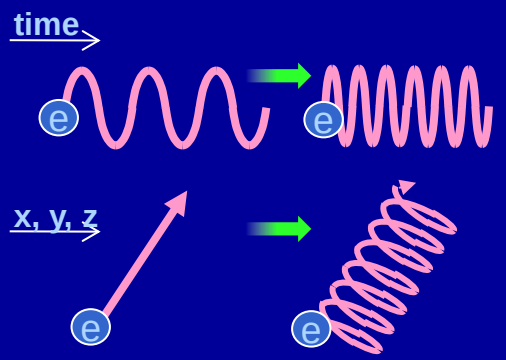
Etching systems

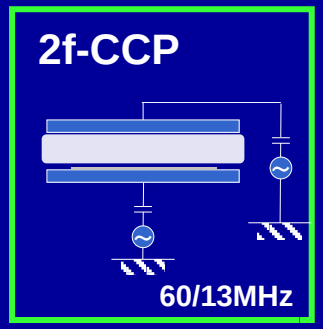




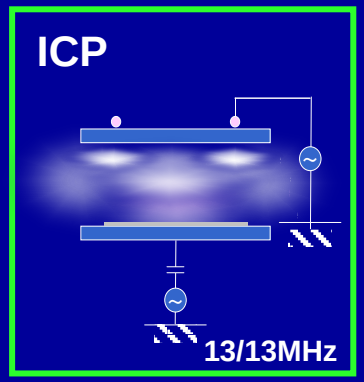
i) Higher frequency

ii) Magnetic field



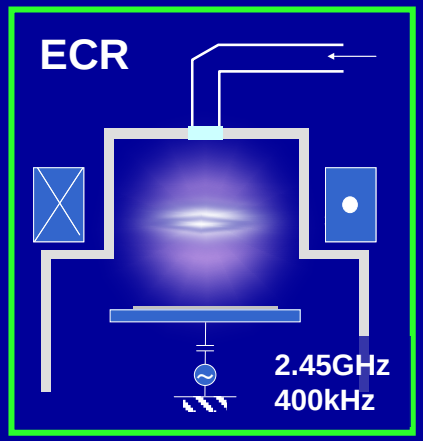


Collision rate↑
(ionization)



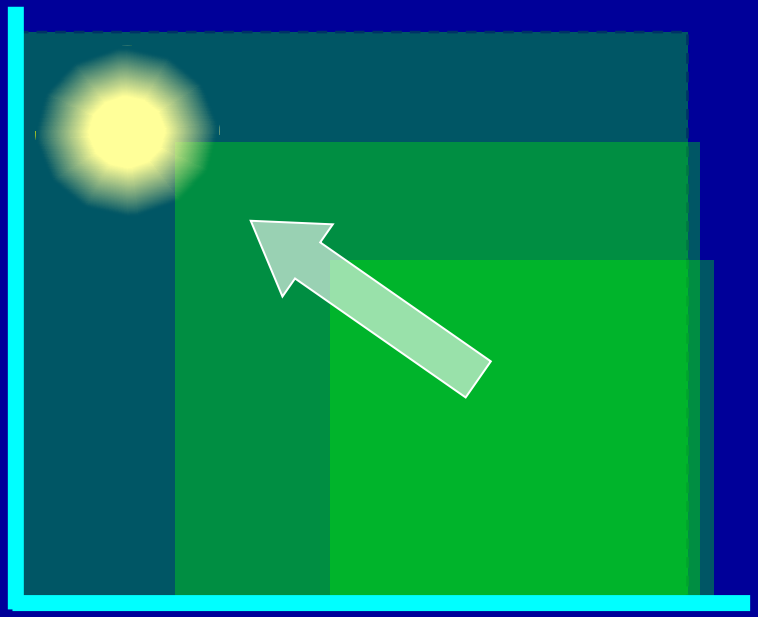
iii) Capacitive
→ Inductive
→ Wave heating

Current loss to walls ↓



High density plasma
Independent control of ion energy

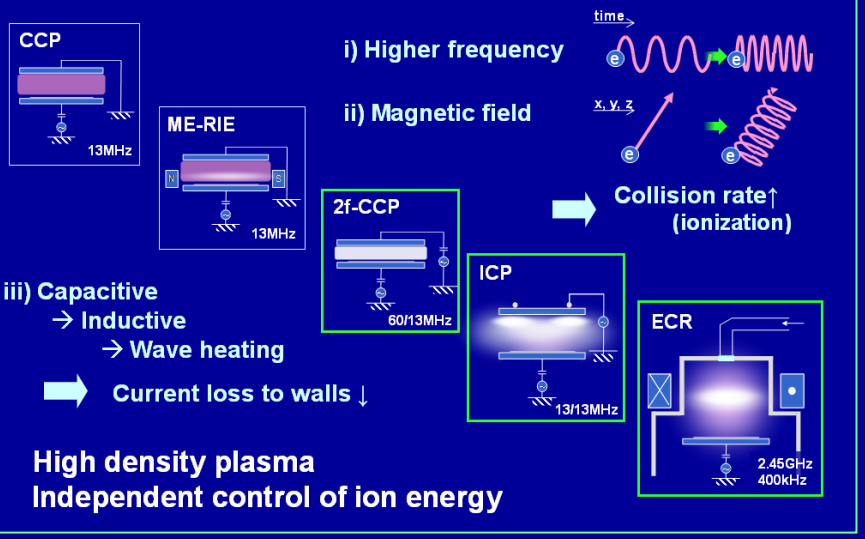
1990～



Vertical profile
High etch rate
High selectivity

HBr/O_2
High density source
Low ion energy

High etch rate



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Requirements (2000～)

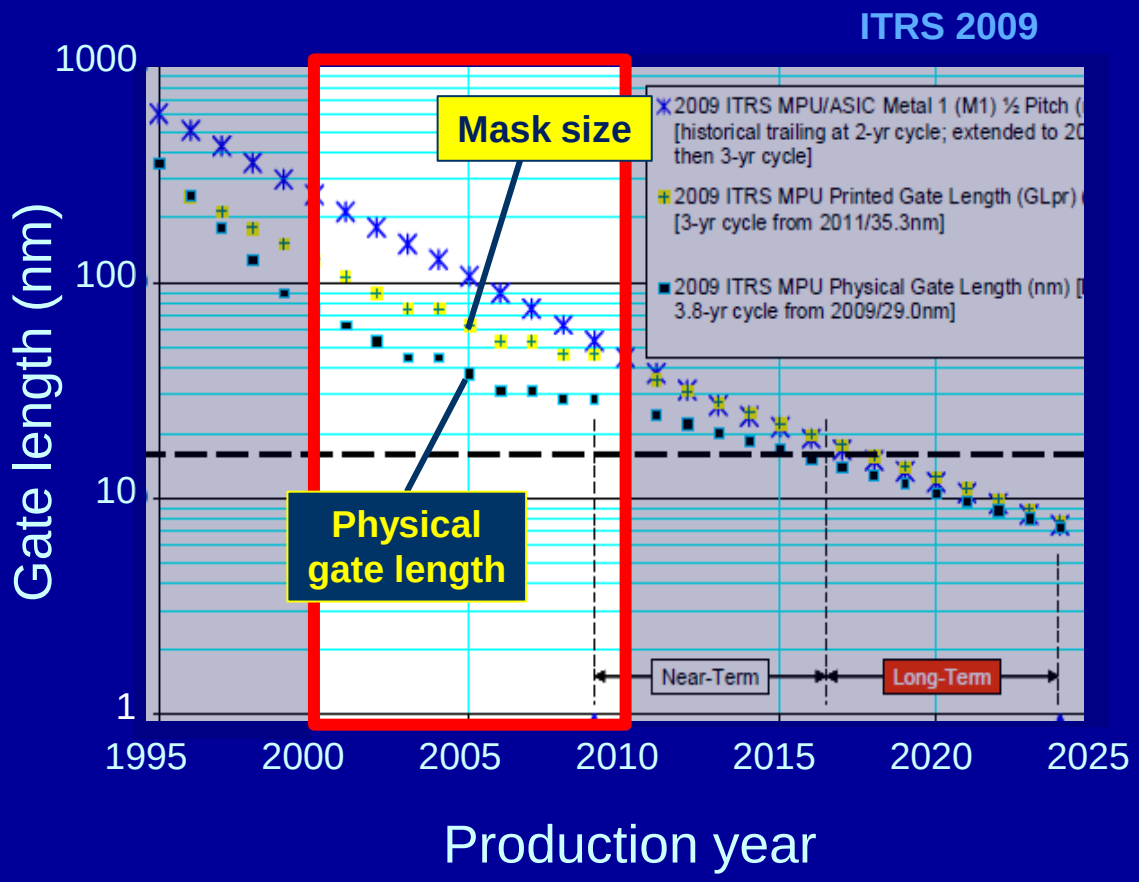
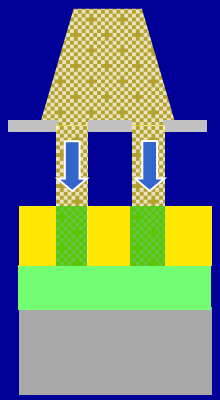


Photo lithography



193nm
(ArF LASER)

Resist mask

Poly-Si

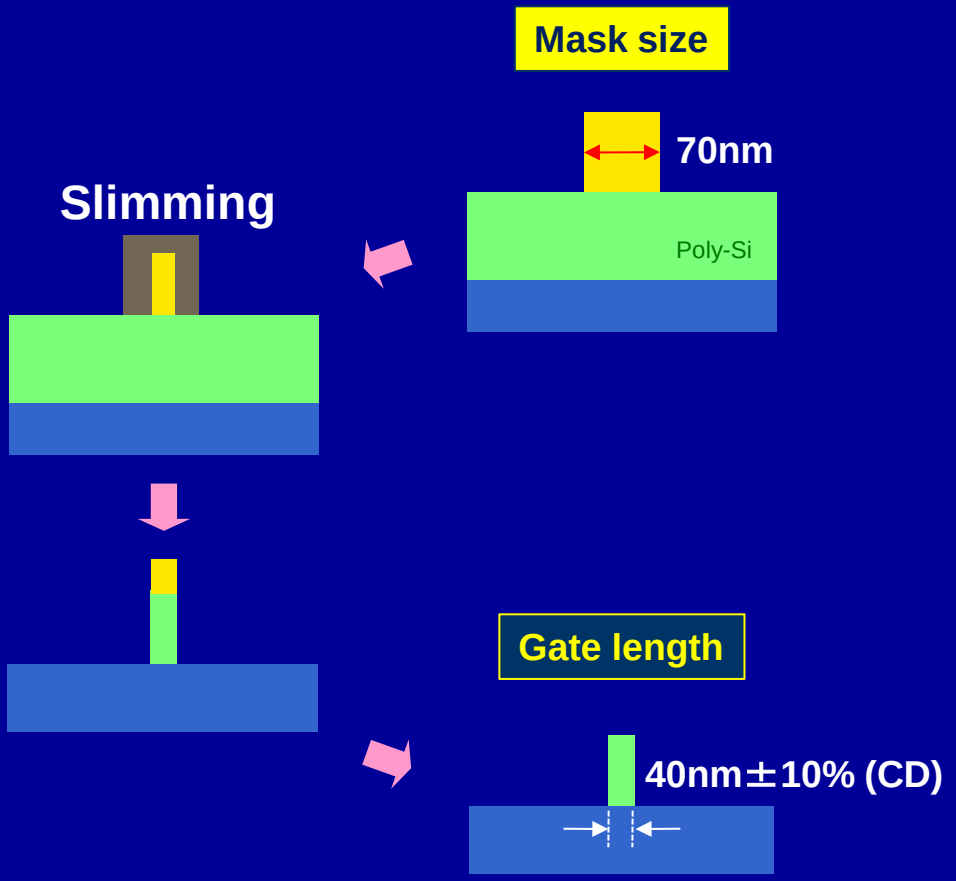
Gate length <100nm
300mmϕ wafer
High etch rate
Anisotropic profile
High selectivity
Uniformity
High-k/Metal Gate

Fluctuation of CD (Critical Dimension)

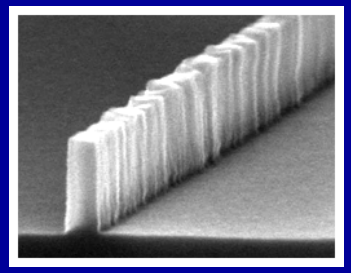
Top view of resist mask

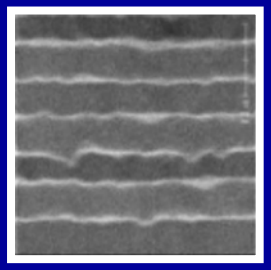
Edge roughness

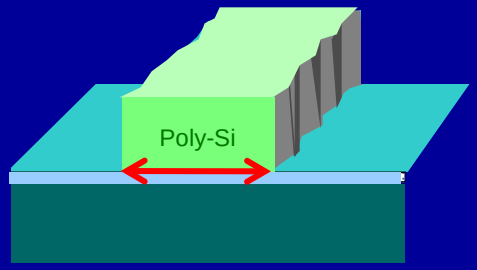
Narrow pattern
Mask roughness



LWR (Line width roughness)

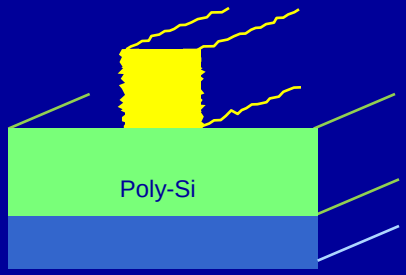


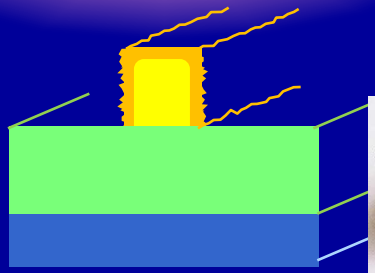


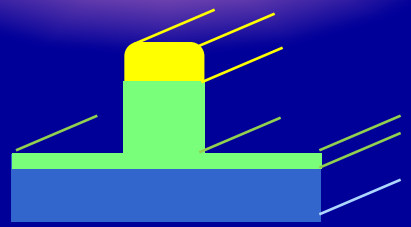


HBr plasma w/o bias

HBr/O_2 plasma w/ bias







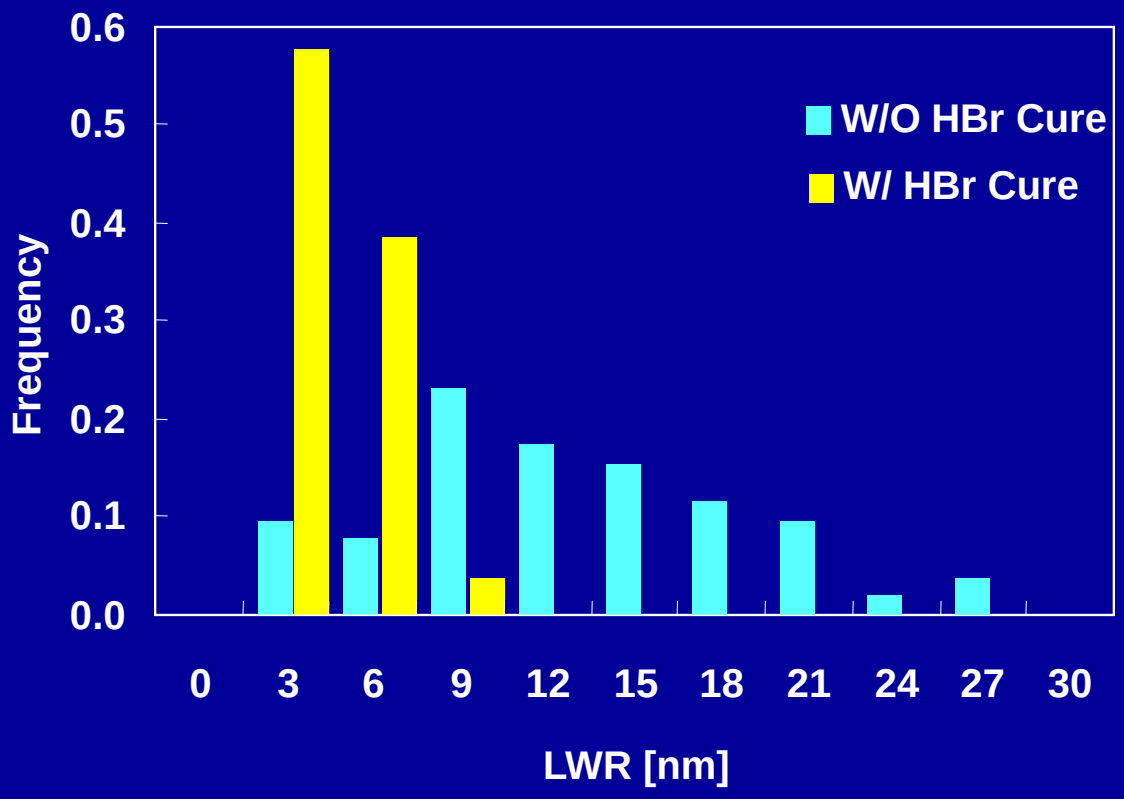
Resist

HBr cure

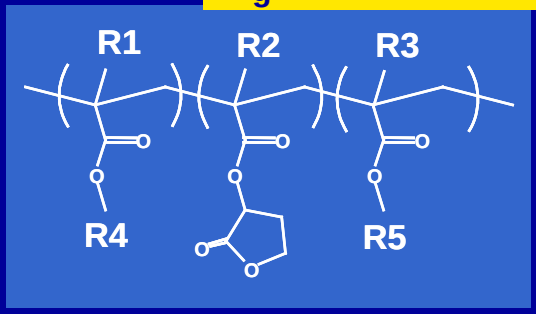
Etching

LWR is improved by HBr plasma cure

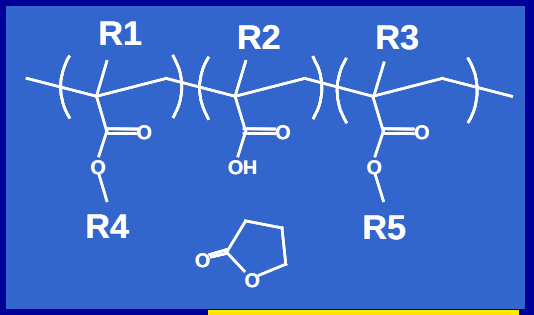
Improvement of LWR



T_g = 402.6 K



HBr cure



T_g = 364.6 K

“Softening” of resist surface by HBr plasma treatment

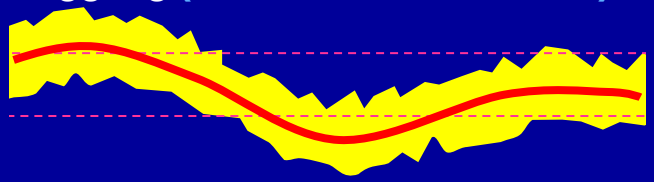
A. Ando, DPS2005 & Thin Solid Films 515 (2007) 4928

Fluctuation of CD (Critical Dimension)

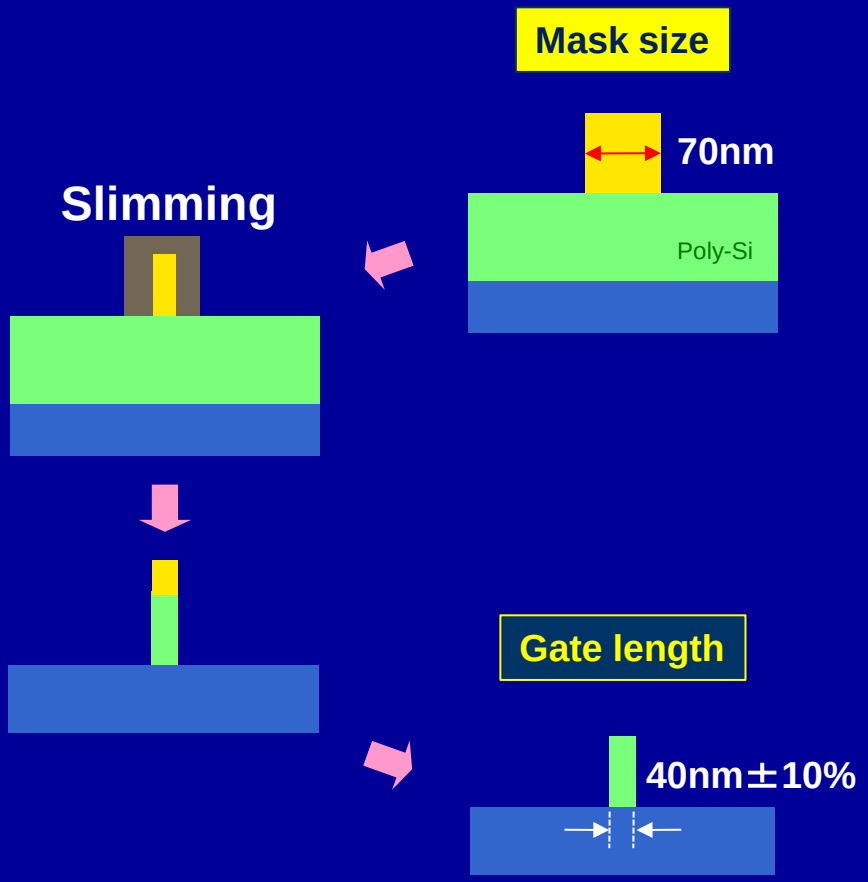
Top view of resist mask

Edge roughness (→Molecular size)

Wiggling (→ Plasma Modification)

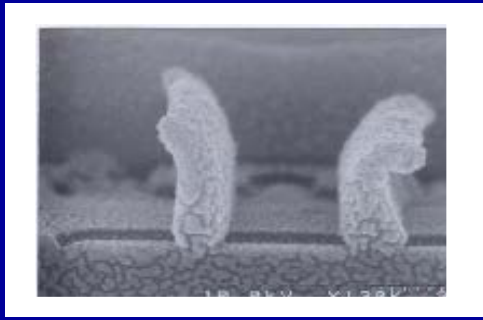


Narrow pattern
Mask roughness



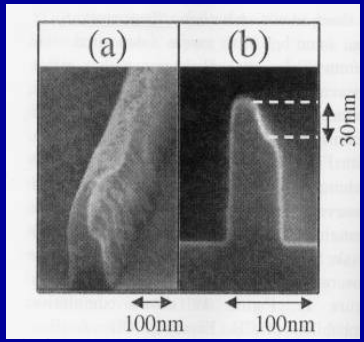
Bending/Wiggling

C-F polymer



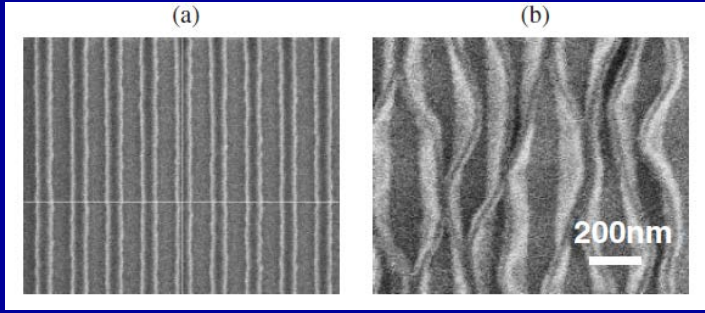
Kurihara, DPS2004

$SiBr_x$



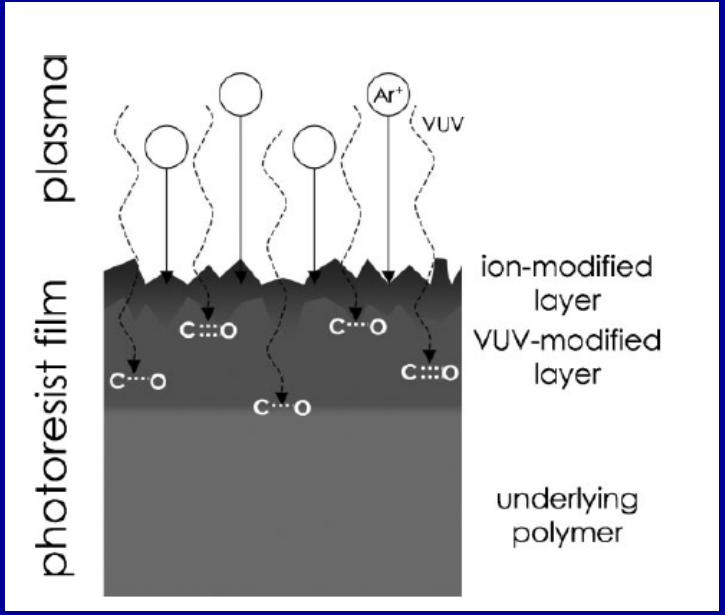
Nagase, DPS2001

Fluorination



I. Sakai, JJAP 46 (2007) 4286

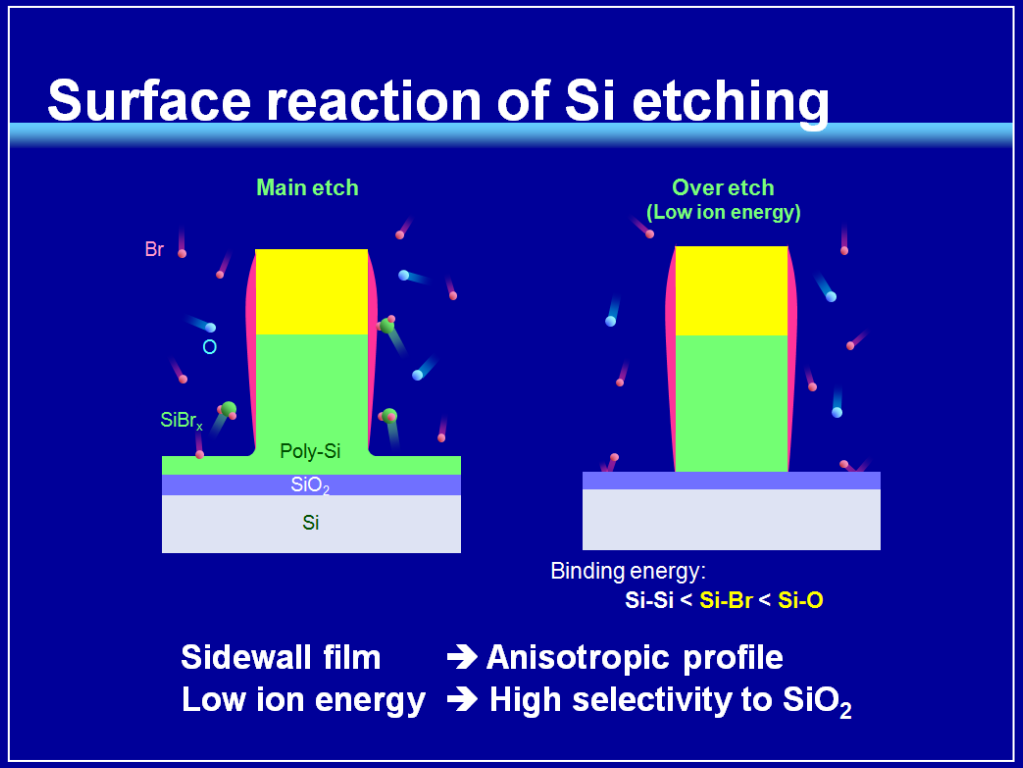
VUV, ion bombardment, and temperature



D. Nest , Plasma Process. Polym. 6 (2009) 649

Stress between softened layer of resist and deposition layer

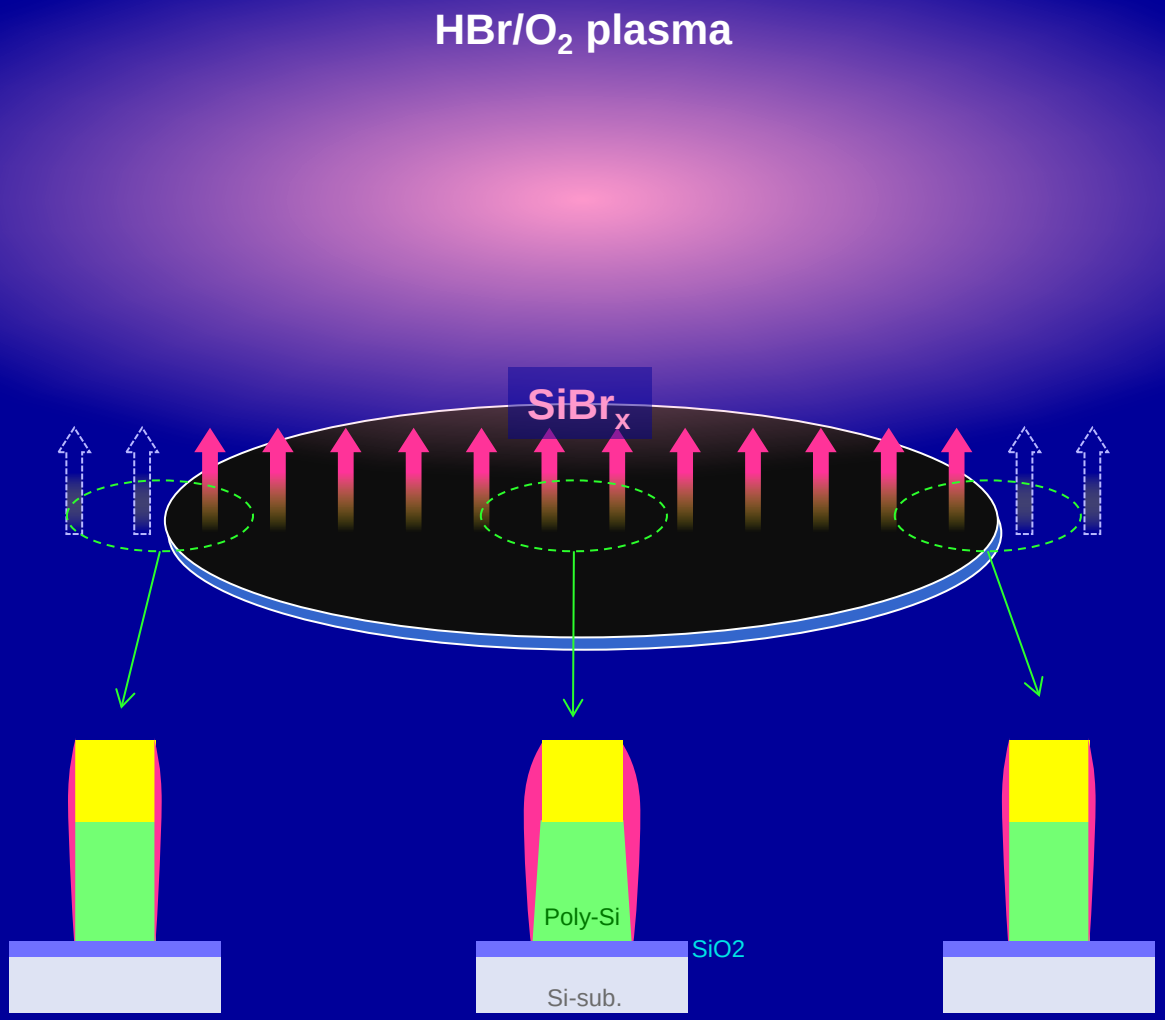
CD non-uniformity within a wafer



Slimming, Surface cure, etc. → Small pattern with less LWR

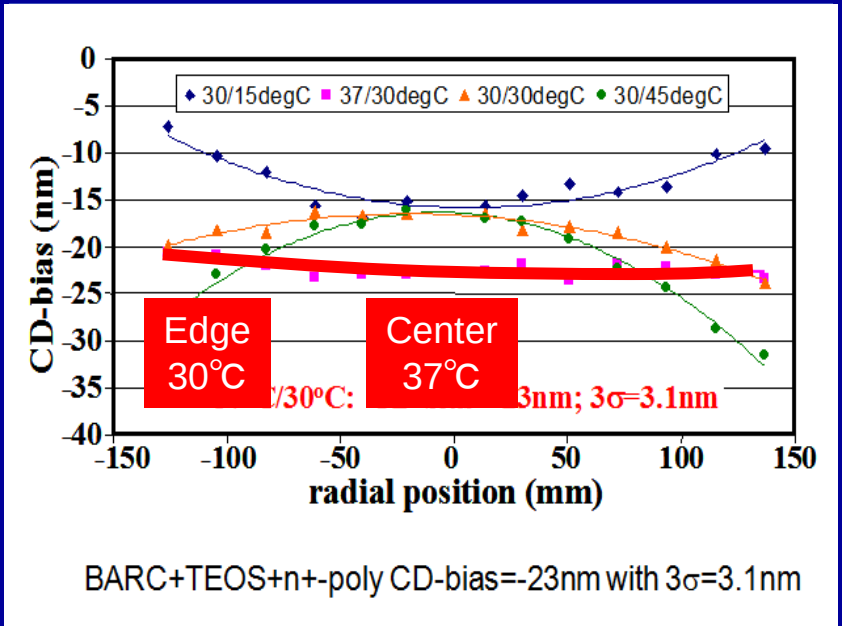
Uniformity within a wafer ?

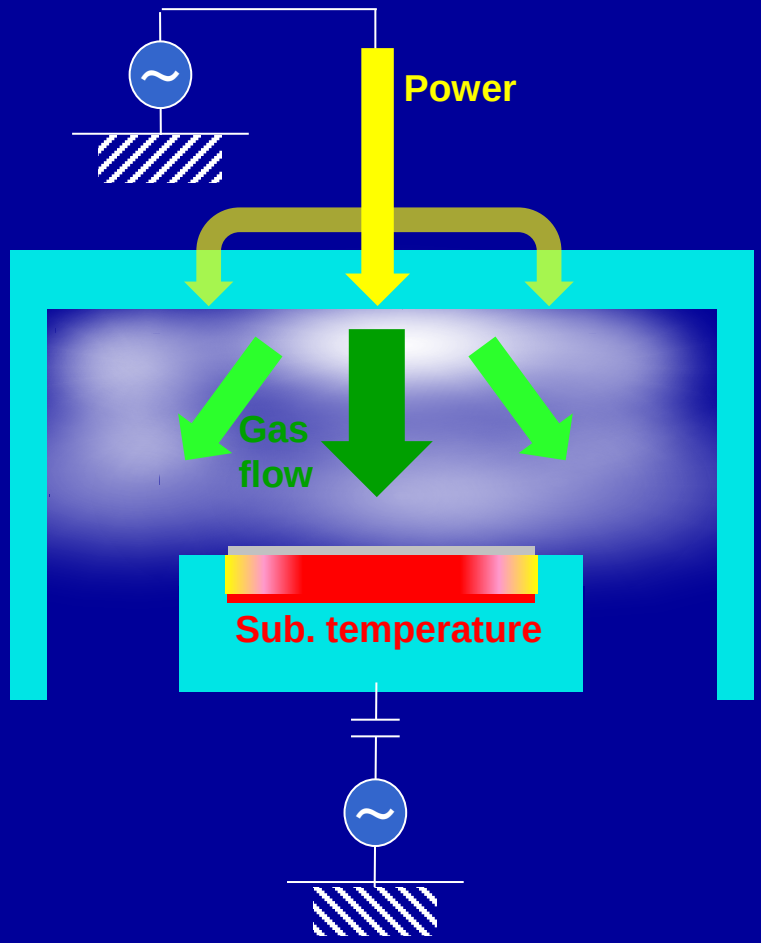
CD non-uniformity within a wafer



Control Knobs

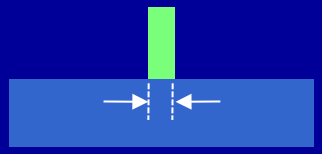
L. Chen, AVS2004





Spatial distribution of Plasma density, Gas flow & Wafer temperature

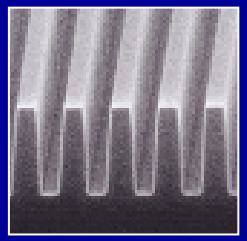
2000~

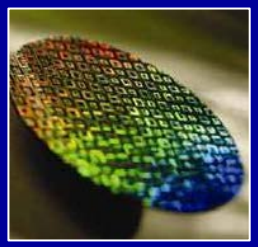


40nm±10%

CD uniformity

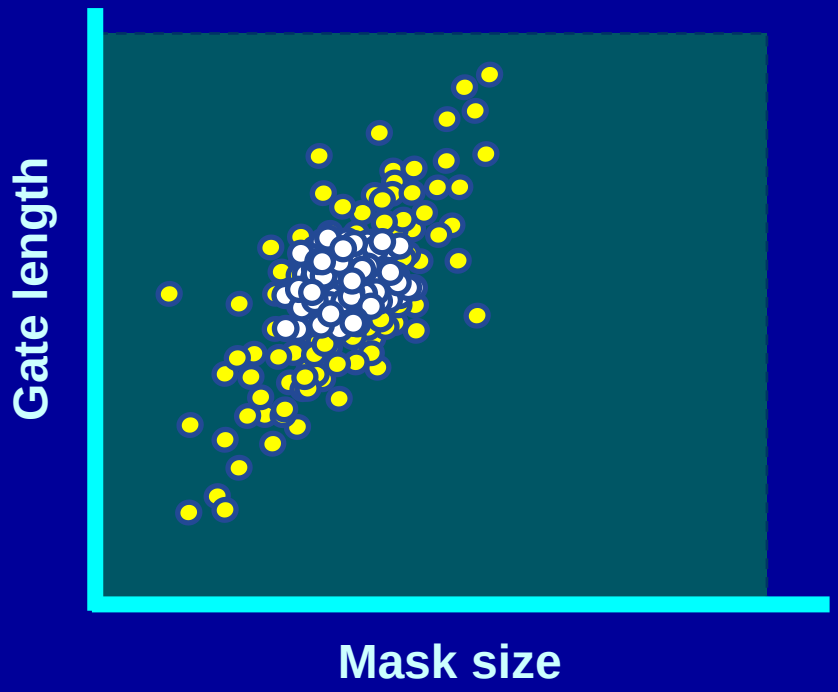
within a chip





within a wafer

within a lot



Plasma cure, Control Knobs, EES

➔ Minimization of CD variation

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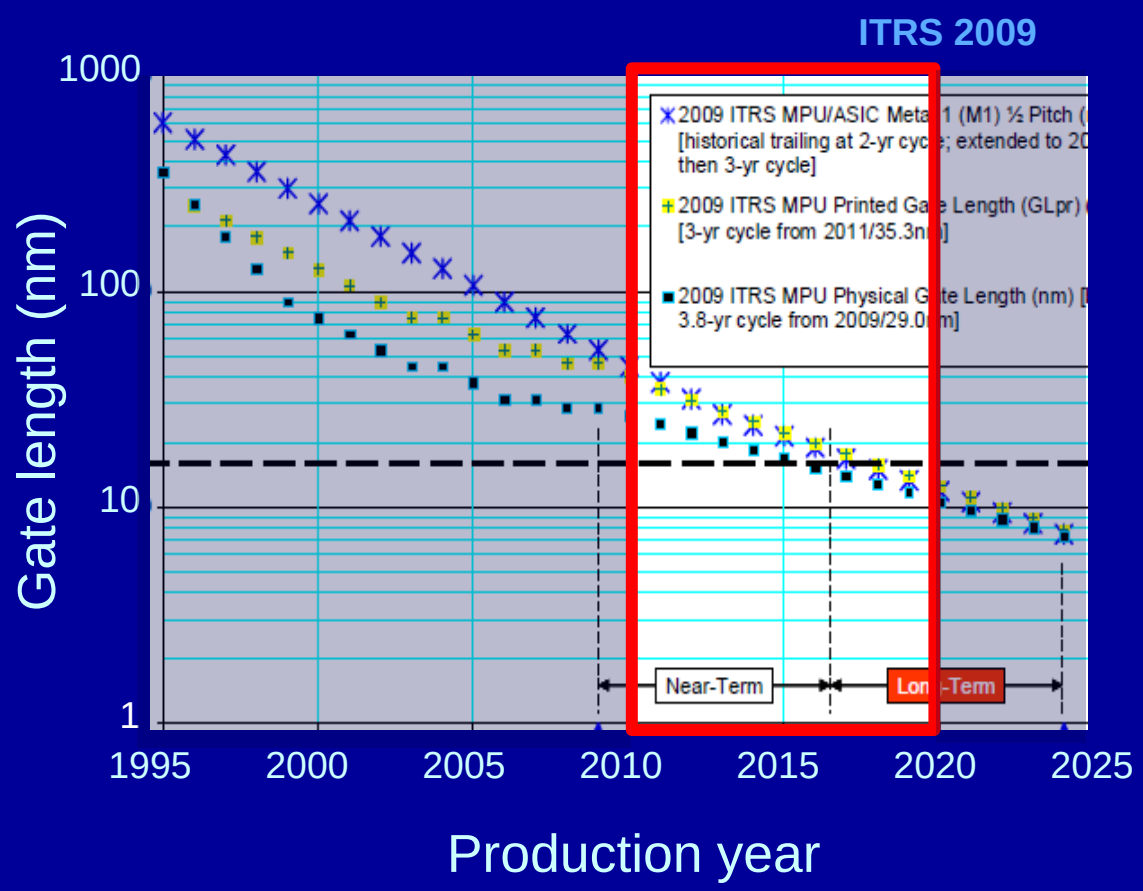
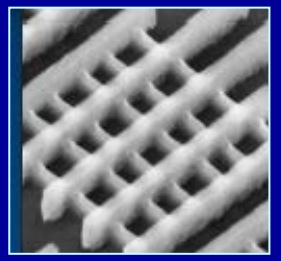
Requirements (2010～)

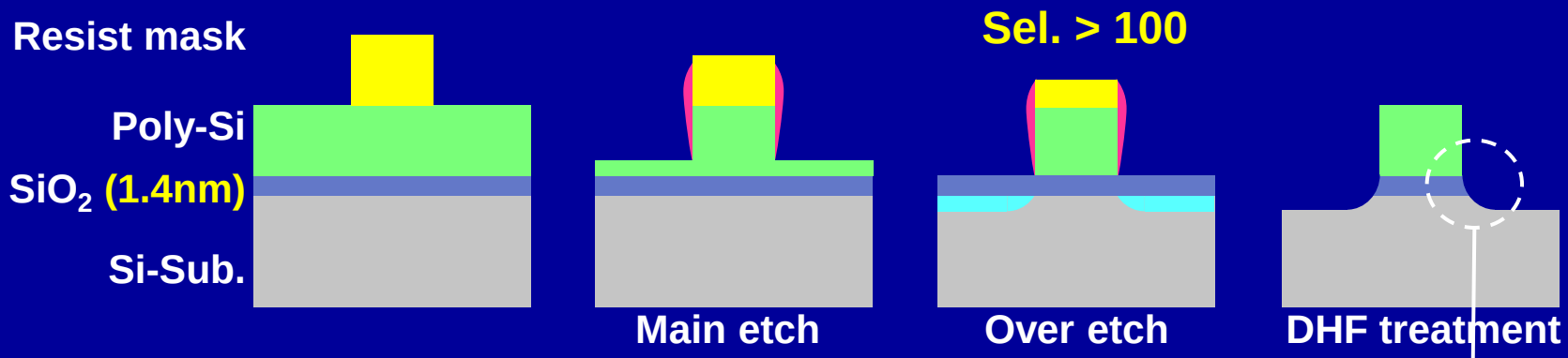


Gate length <30nm
Less damage
450mmΦ wafer
High etch rate
Anisotropic profile
High selectivity
Uniformity
High-k/Metal gate
Fin transistor



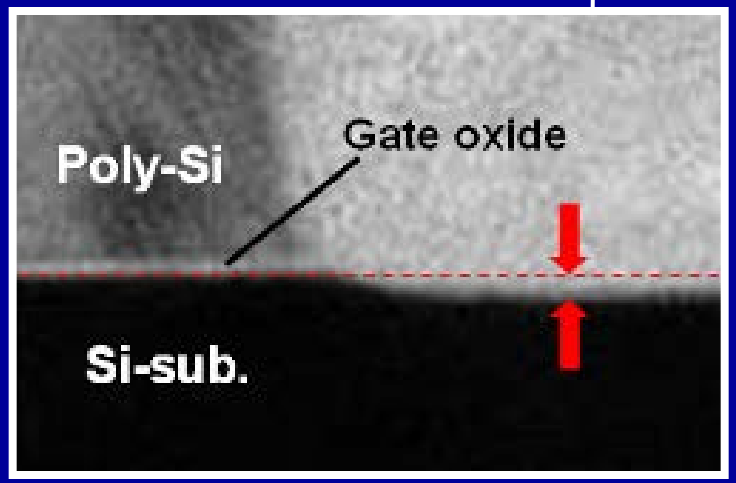
http://www.intel.co.jp

Si recess



Damaged layer formed during gate etching

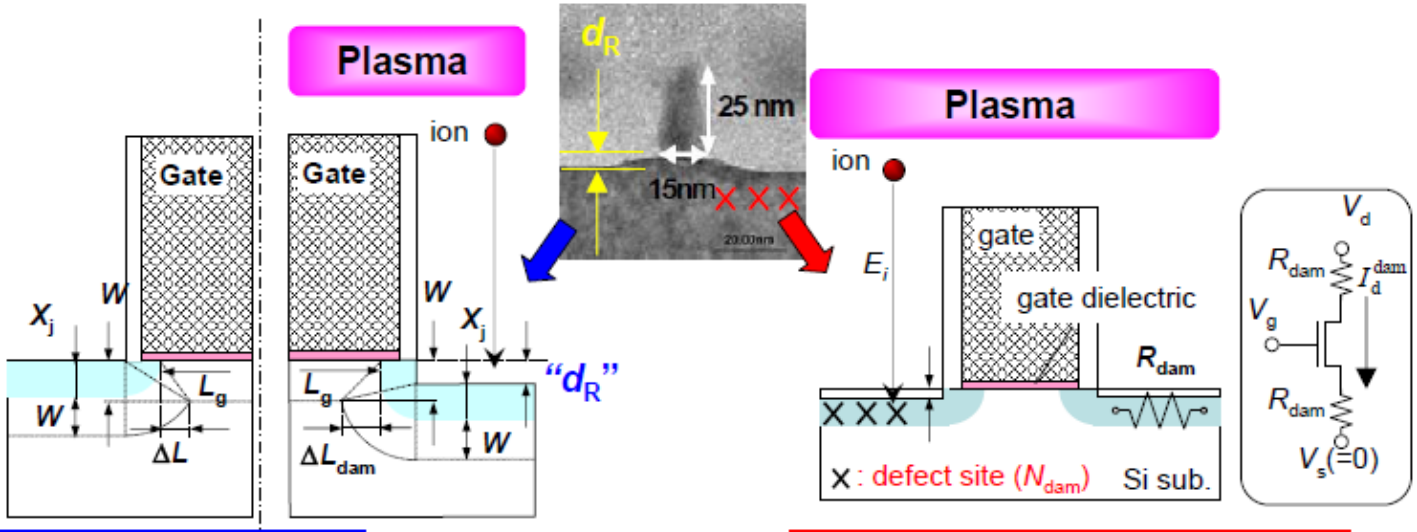
(High selectivity ≠ Less Damage)



T. Ohchi., JJAP 47 (2008) 5324

Si recess

Analytical Models – Effects of Si recess and Defect Site



V_{th} shift by d_R

$$\Delta V_{th} \approx -\frac{qN_A W}{C_{ox} L_g}\left(\frac{W}{\sqrt{X_j^2 + 2WX_j}} d_R\right)$$

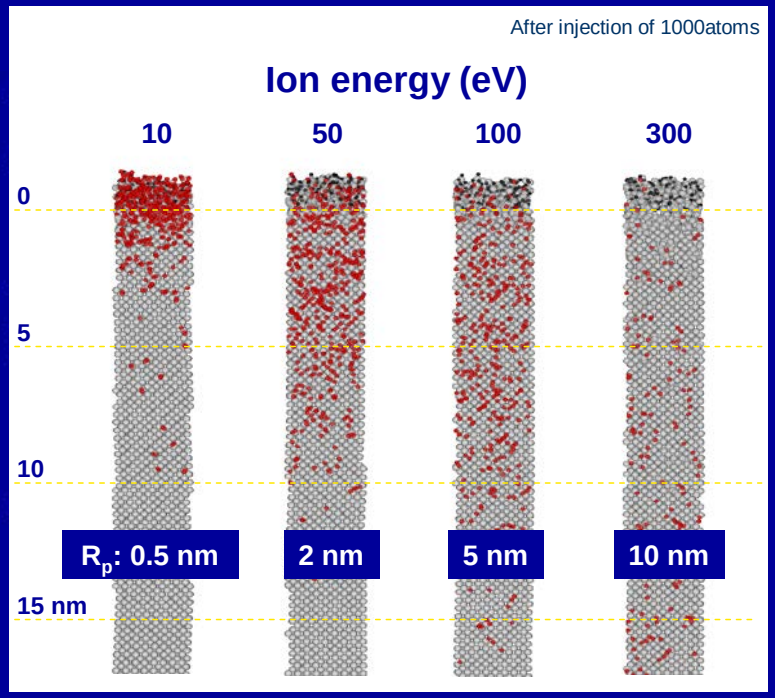
I_d degradation by N_{dam}

$$I_d^{dam} \approx \frac{\beta' V_d}{2A\beta' + n_0}\left(n_0 - \frac{2A\beta'}{2A\beta' + n_0} N_{dam}\right)$$

K. Eriguchi et al., IEEE EDL 30 (2009) / 31 (2009).

Si recess induces fluctuation of V_{th} or I_d

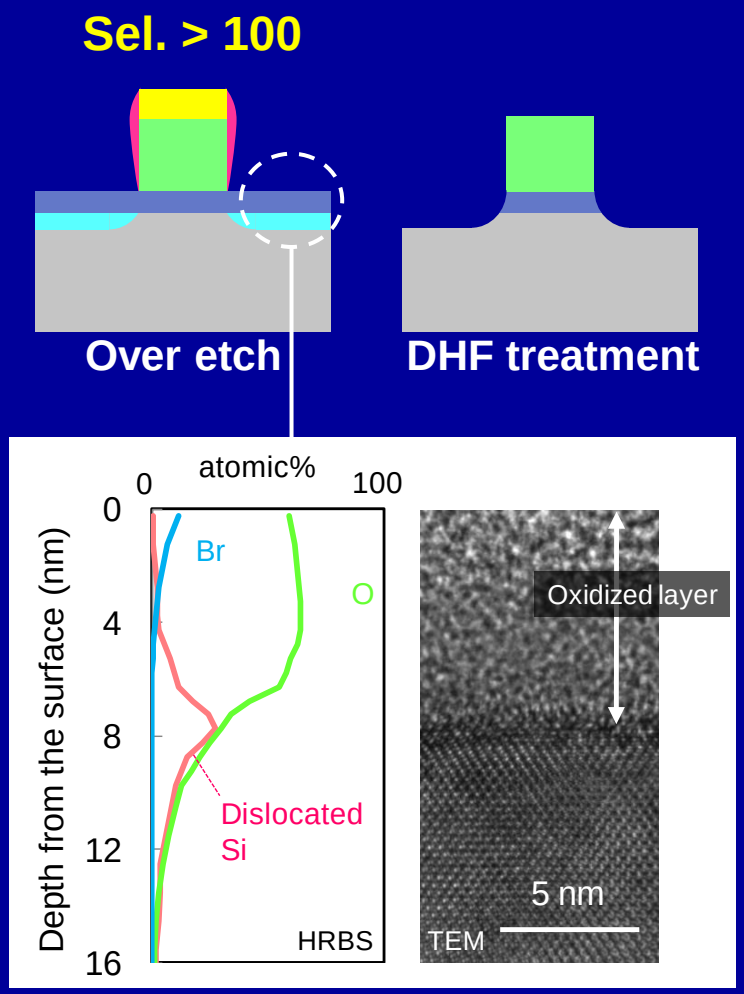
Si recess



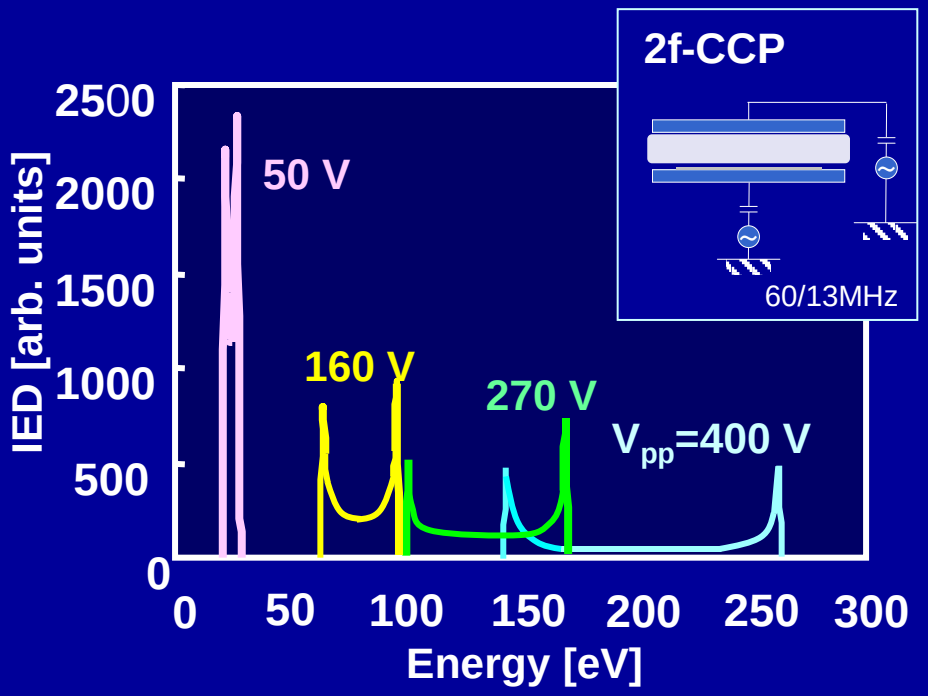
Damaged layer formed during gate etching

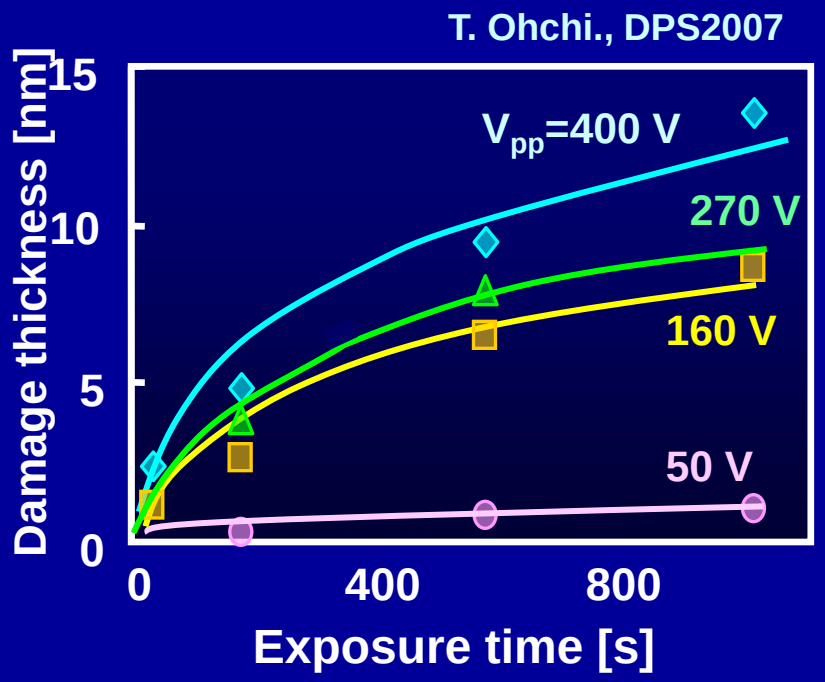
(High selectivity ≠ Less Damage)

HBr ?



Suppression of Si recess



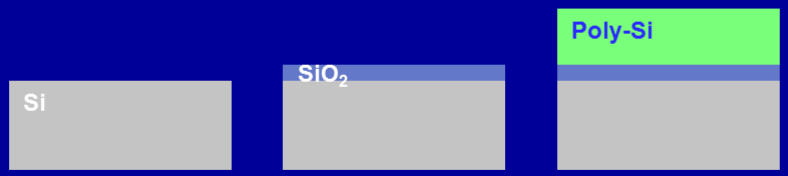


Quantitative control of IEDF

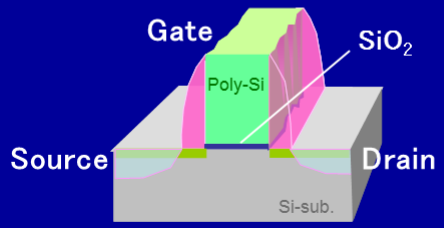
➔Minimization of ion induced damage

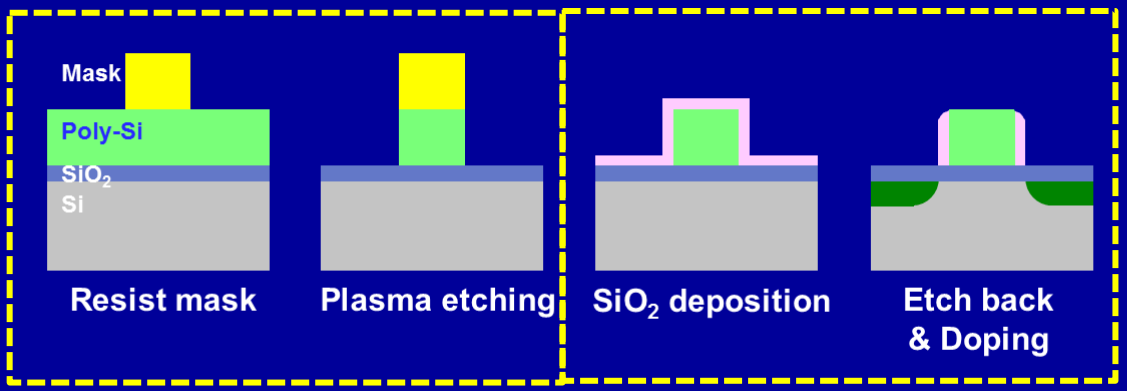
Sidewall etching

Fabrication process



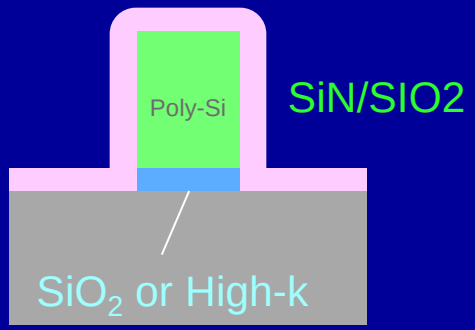
Si-substrate | Gate SiO_2 | Doped poly-Si

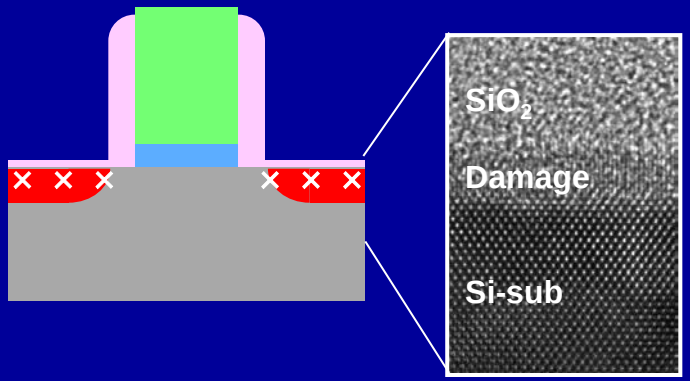


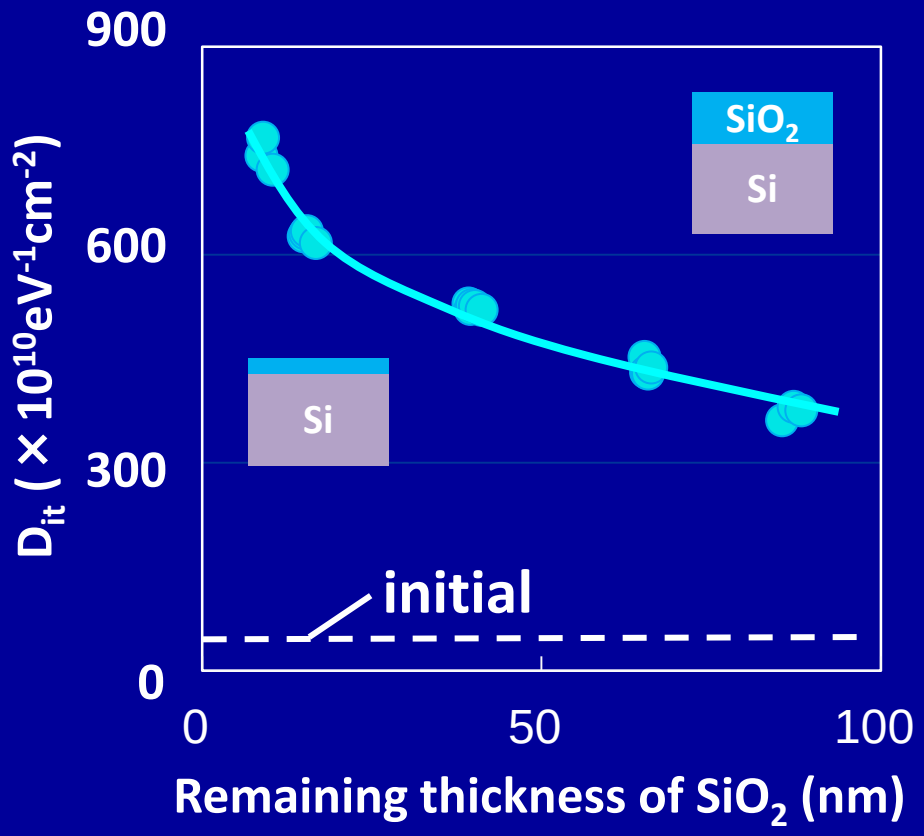


Resist mask | Plasma etching | SiO_2 deposition | Etch back & Doping

Sidewall etching



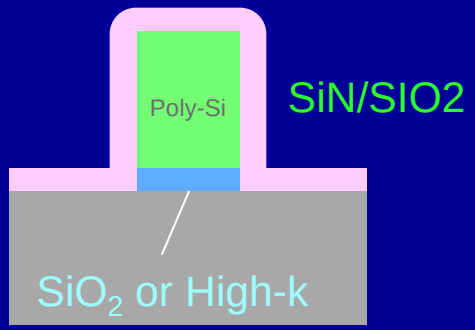


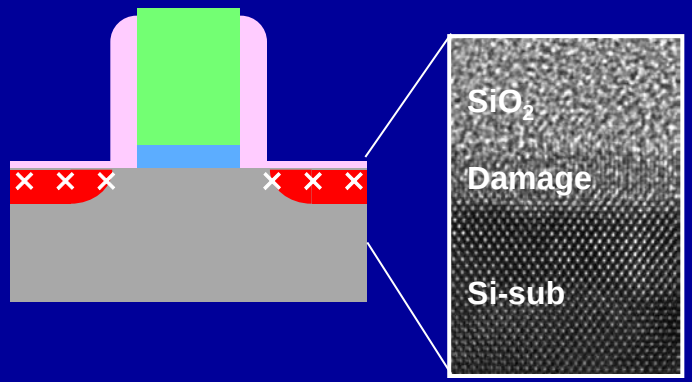


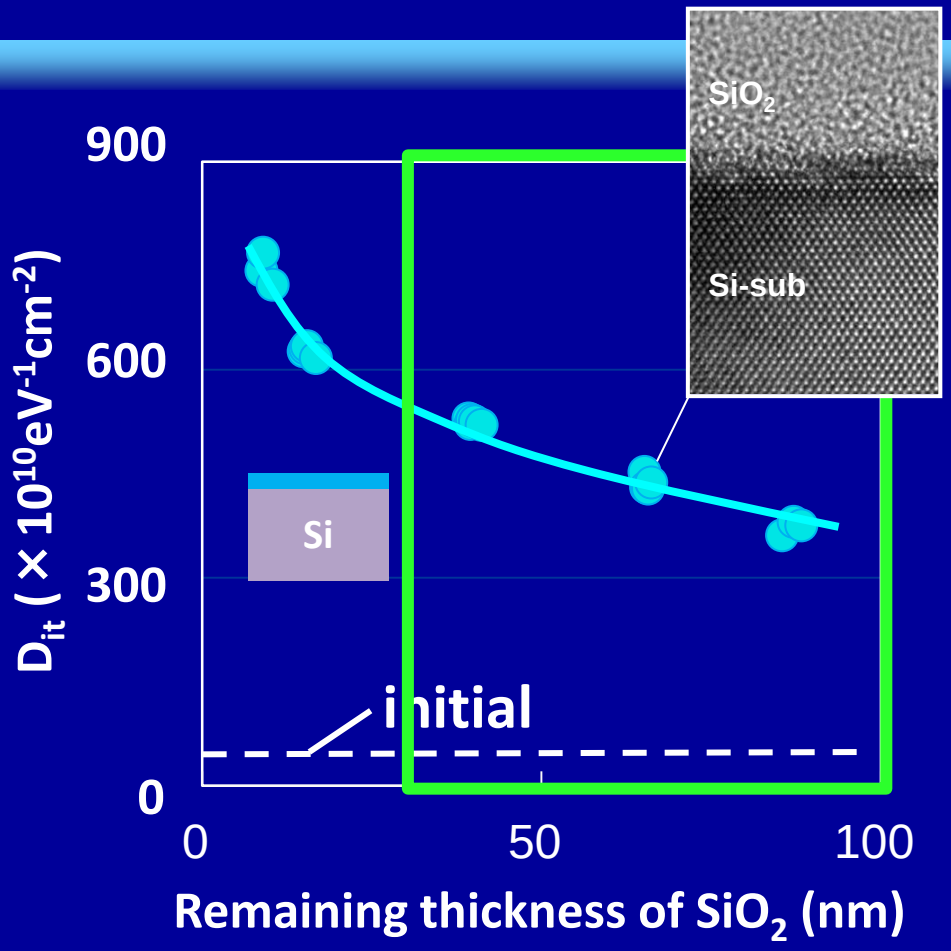
D_{it} caused by Ion or Photon

D_{it}: Interface trap density

Sidewall etching



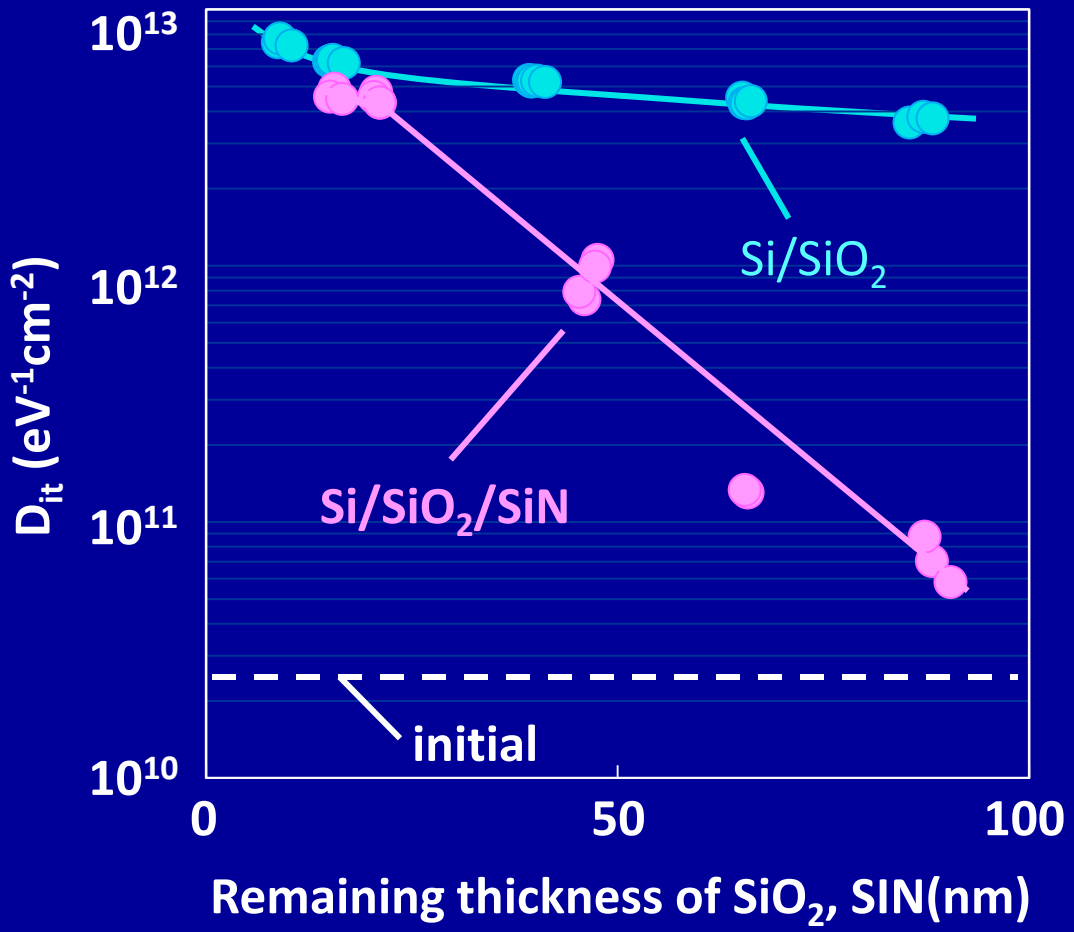


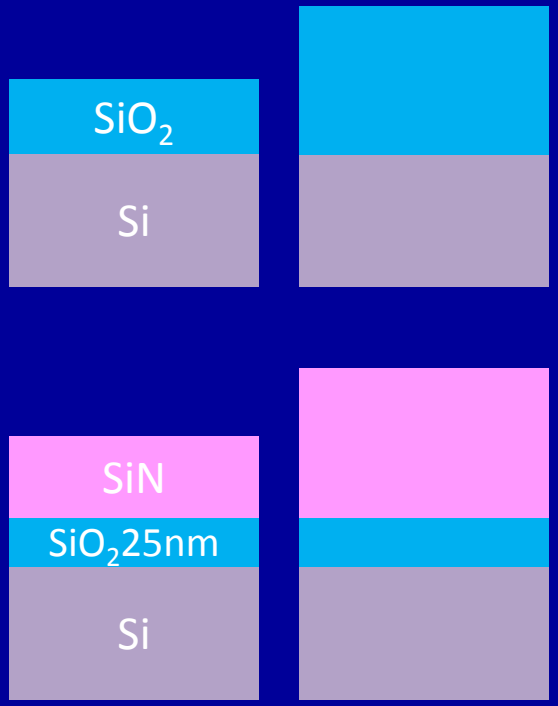


D_{it} caused by Ion or Photon

D_{it}: Interface trap density

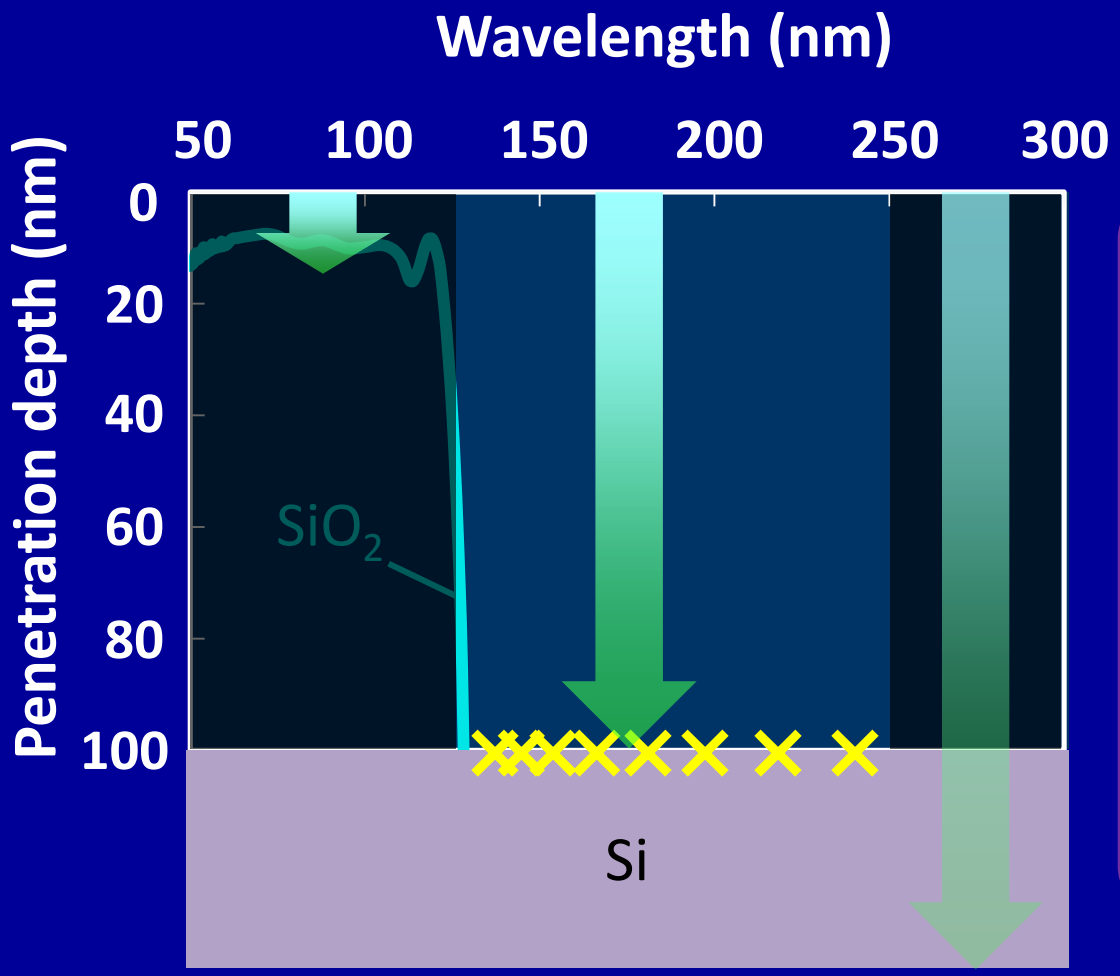
Damage at SiO_2/Si interface

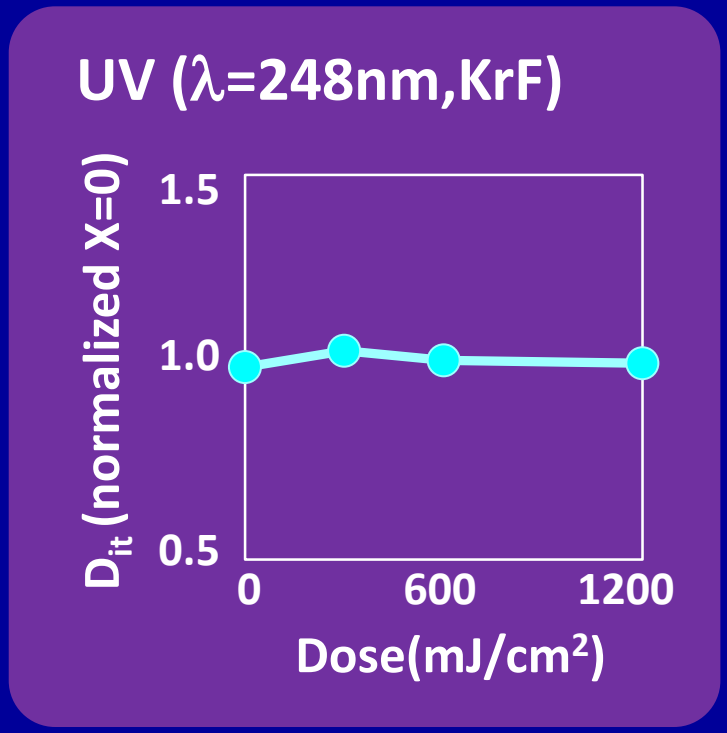




D_{it} (SiN) < D_{it} (SiO_2)

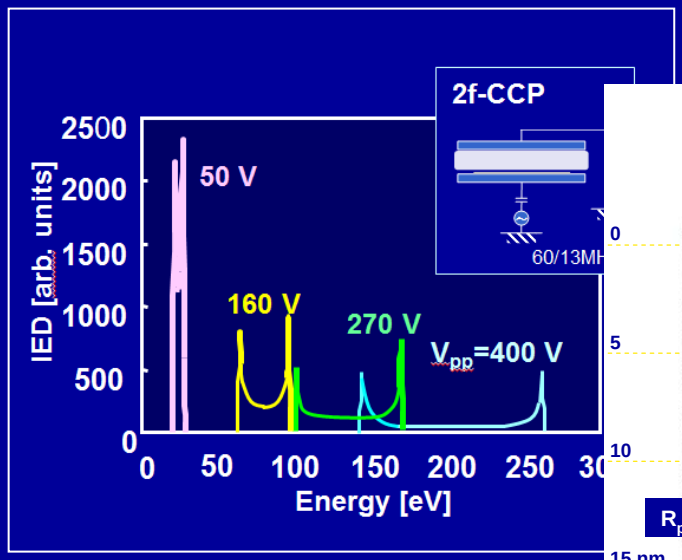
UV induced damage

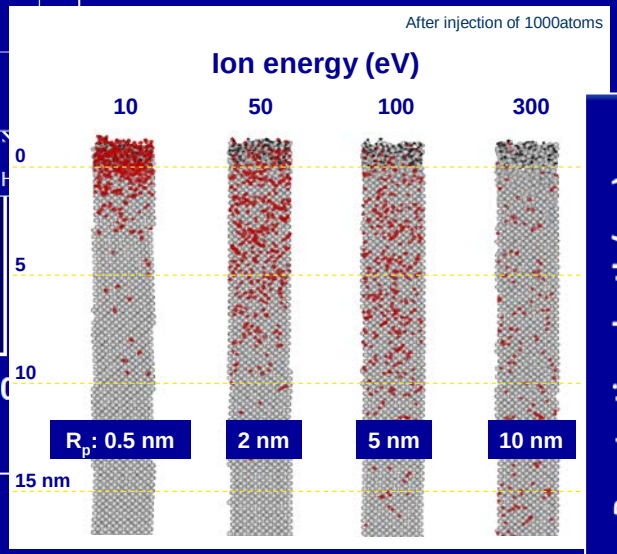


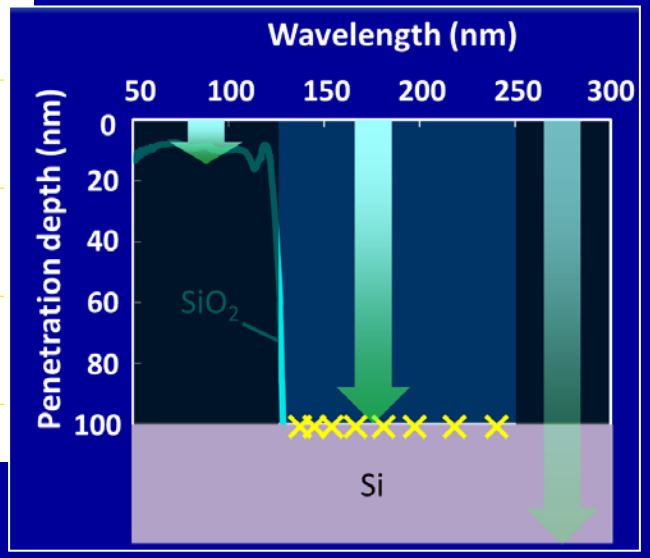


VUV is absorbed at top surface of SiO_2 (or SiN)

2010～



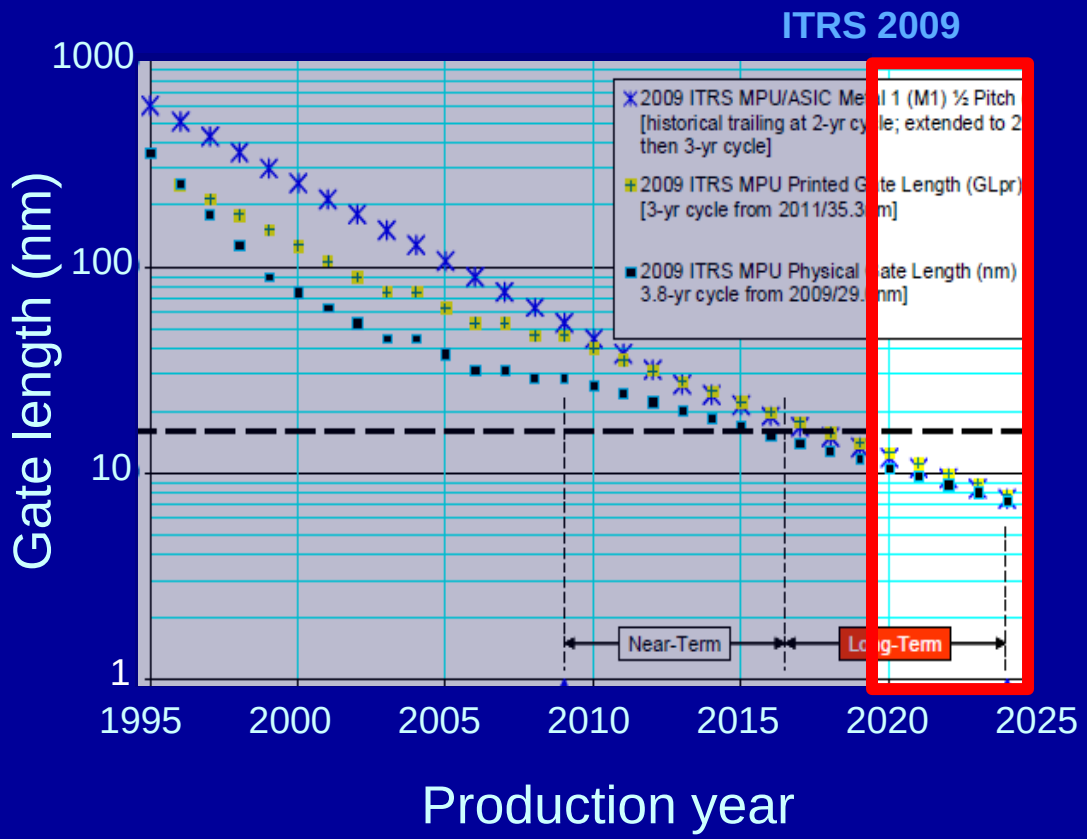




Quantitative control of IEDF
Prediction of ion and UV/VUV penetration

➔ **Minimization of physical & radiation damage**

2020～（？）

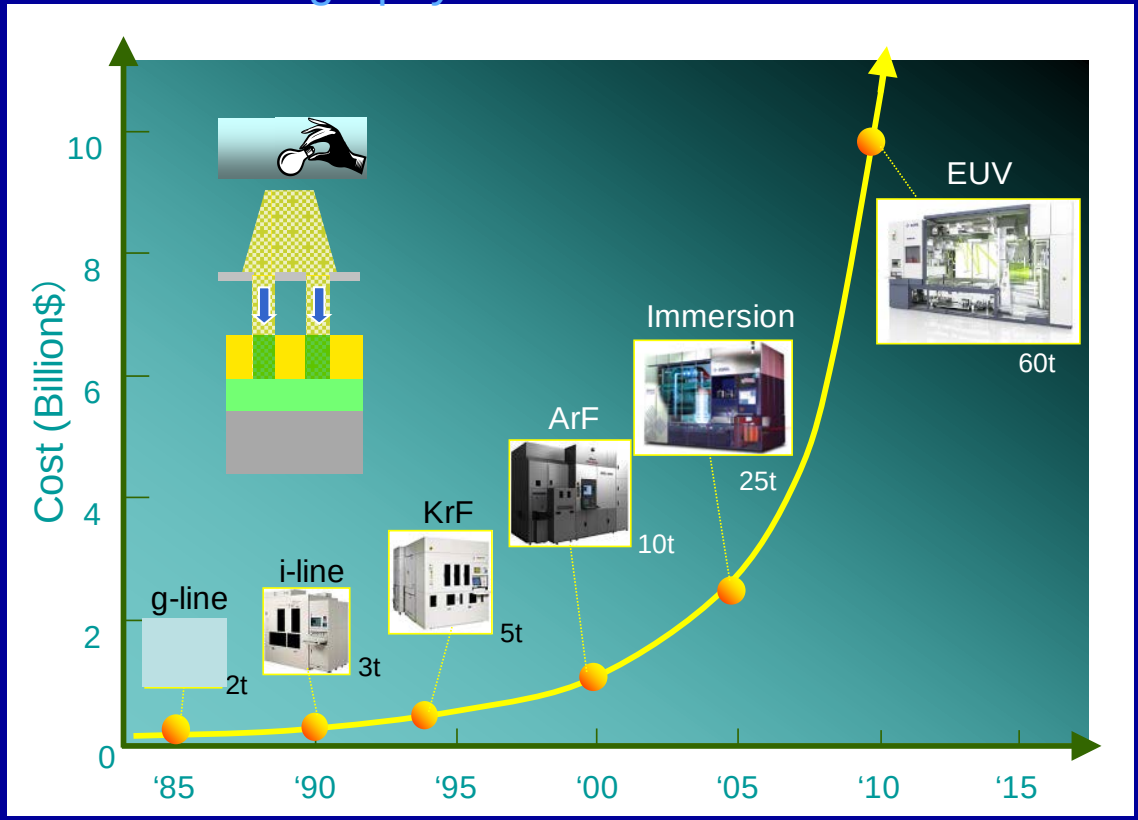


Miniaturization limit ?

Gate length <10nm?
Less damage
450mmΦ wafer
High etch rate
Anisotropic prpfile
High selectivity
Uniformity
High-k/Metal gate
Fin transistor
3D
CNT/Graphene
Spin device・・・

Further miniatuarization

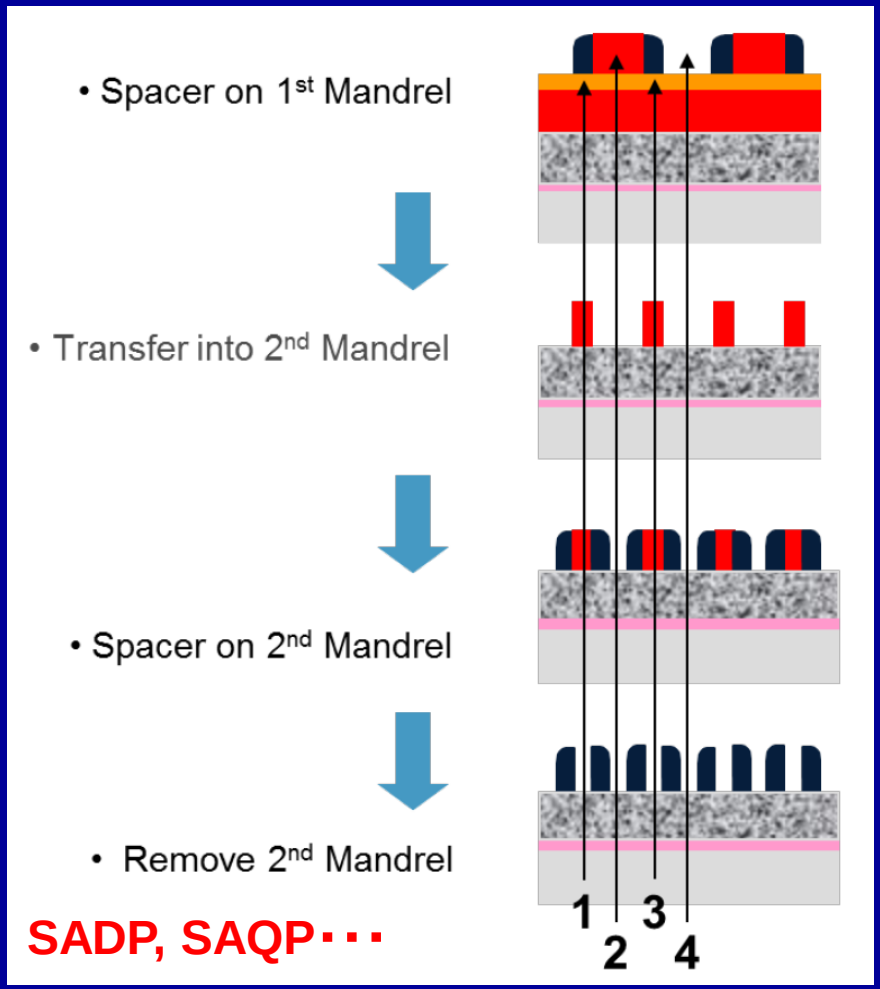
Price of Lithography tools



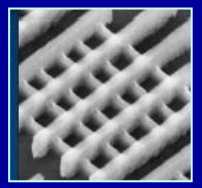
Cost limit ?

Further miniatuarization

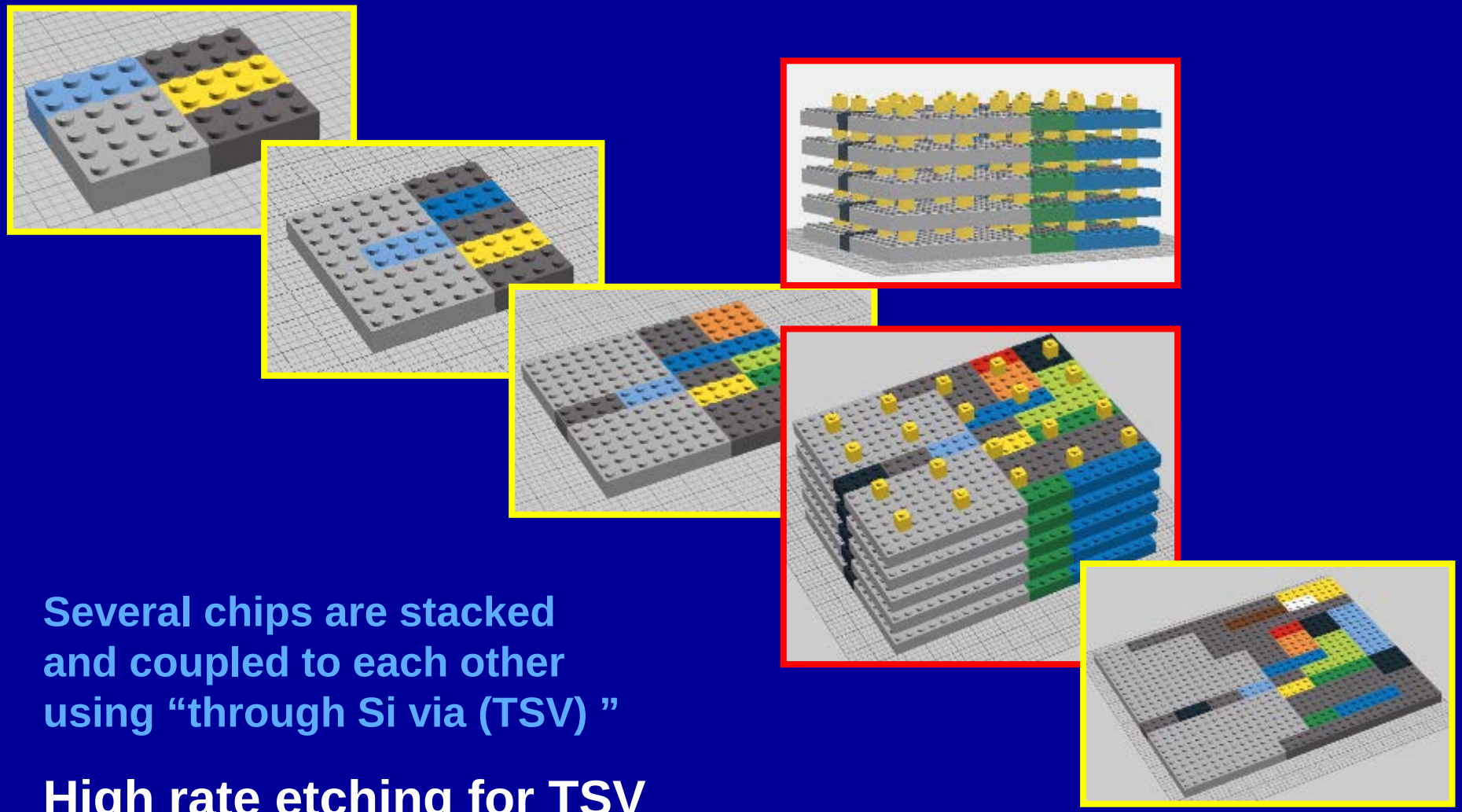
ITRS
2013



Self-Aligned Double/Quadra Patterning



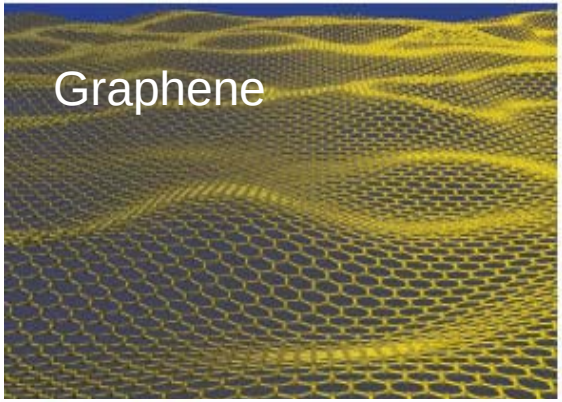
3D LSI

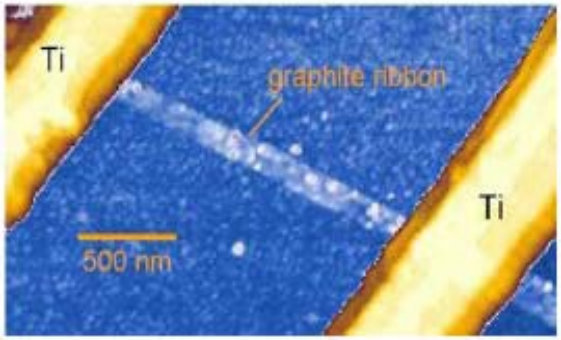


Several chips are stacked and coupled to each other using “through Si via (TSV) ”

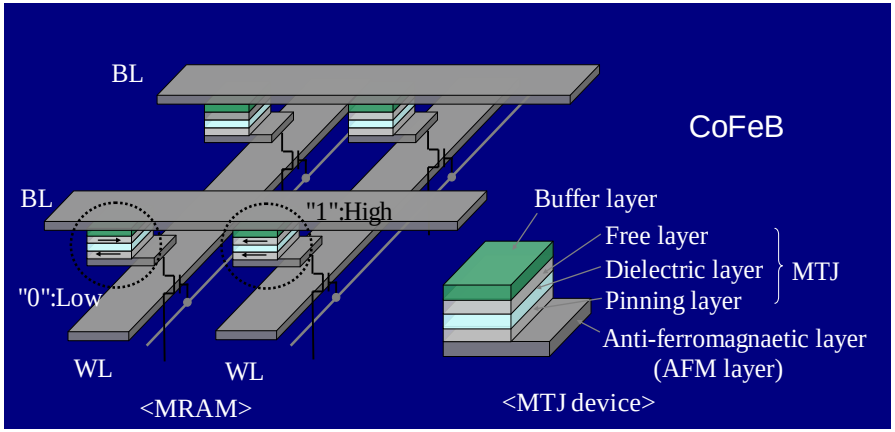
High rate etching for TSV

New device, New materials





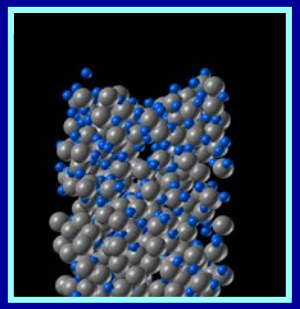
Carbon electronics
(CNT, graphene)



MRAM / Spin electronics
(Ferromagnetic materials)

New requirement for plasma process & system

Toward future device fabrication



Control ?

Monitoring ?

Prediction ?

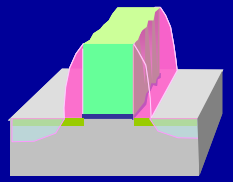
Data base ?

Quantitative understanding of plasma and surface reactions

Quantitative manipulation of electrons, ions and photons

➔ **Fine pattern, TSV, New materials & structures**

Summary



1990～ **High etch rate & Selectivity**

- **HBr/O_2**
- **High density / low ion energy plasma**

2000～ **Suppression of CD fluctuation**

- **Suppression of LWR and Wiggling of mask**
- **Knobs for plasma uniformity control**

2010～ **Minimization of plasma induced damage**

- **IEDF control, UV/VUV control**
- **Advanced monitoring & simulation**

2020～ **New plasma processes for future devices**

- **Quantitative control of electrons, ions and photons**